

- ## N73Sv Block Diagram





PCH GPIO

PCH IBEX GPIO	Use As	Signal Name	Int.& Ext Pull up / down	Power
GPIO 00	GPO	NC_TP	-	+3VS
GPIO 01	GPO	NC_TP	-	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#	EXT PU	+5VS
GPIO 06	GPI	NC_TP	EXT PU	+3VS
GPIO 07	GPI	USB3_SMI#	EXT PU	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	NC_PU	EXT PU	+3VSUS
GPIO 10	Native	NC_PU	EXT PU	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS
GPIO 12	Native	NC_TP	-	+3VSUS
GPIO 13	GPO	NC_TP	INT PD	+3VSUS
GPIO 14	Native	NC_PU	EXT PU	+3VSUS
GPIO 15	GPO	BT_LED	INT PD	+3VSUS
GPIO 16	GPO	DGPU_HOLD_RST#	EXT PU	+3VS
GPIO 17	GPI	DGPU_PWROK	EXT PD & INT TBD	+3VS
GPIO 18	GPI	CLKREQ1_TV#	EXT PD	+3VS
GPIO 19	GPI	SATA0GP	EXT PU	+3VS
GPIO 20	Native	CLKREQ2_WLAN#	EXT PD	+3VS
GPIO 21	GPI	SATA0GP	EXT PU	+3VS
GPIO 22	GPO	WLAN_LED	-	+3VS
GPIO 23	Native	NC_TP	INT PU	+3VS
GPIO 24	GPO	NC_TP	-	+3VSUS
GPIO 25	GPI	CLKREQ3_NEWCARD#	EXT PD	+3VSUS
GPIO 26	GPI	CLKREQ4_USB3#	EXT PD	+3VSUS
GPIO 27	GPO	NC_TP	INT PU	+3VSUS
GPIO 28	GPO	WLAN_ON#	-	+3VSUS
GPIO 29	Native		-	+3VSUS
GPIO 30	GPO	ME_SusPwrDnAck	EXT PU	+3VSUS
GPIO 31	Native	ME_AC_PRESENT_PCH	EXT PU	+3VSUS
GPIO 32	GPIO	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	GPI	HDA_DOCK_EN#	-	+3VS
GPIO 34	Native	NC_TP	-	+3VS
GPIO 35	GPI	SATA_CLK_REQ#_R	EXT PD	+3VS
GPIO 36	GPO	DGPU_PWR_EN#	EXT PD	+3VS
GPIO 37	GPI	DGPU_PRSENT#	EXT PD	+3VS
GPIO 38	GPI	PCB_ID0	EXT PU / PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PU / PD	+3VS
GPIO 40	Native	NC_PU	EXT PU	+3VSUS
GPIO 41	Native	NC_PU	EXT PU	+3VSUS
GPIO 42	Native	NC_PU	EXT PU	+3VSUS
GPIO 43	Native	NC_PU	EXT PU	+3VSUS
GPIO 44	Native	CLK_REQ5#	EXT PU	+3VSUS
GPIO 45	Native	NC_TP	-	+3VSUS
GPIO 46	Native	NC_TP	-	+3VSUS
GPIO 47	GPI	CLKREQ_PEG#	EXT PD	+3VSUS
GPIO 48	GPO	NC_TP	-	+3VS
GPIO 49	GPO	PCH_TEMP_ALERT#	EXT PU	+3VS
GPIO 50	Native	PCI_REQ1#	EXT PU	+5VS
GPIO 51	Native	PCI_GNT1#	INT PU	+3VS
GPIO 52	GPO	DGPU_SELECT#_R	EXT PU	+5VS
GPIO 53	GPO	DGPU_PWM_SELECT#_R	INT PU	+3VS
GPIO 54	Native	PCI_REQ3#	EXT PD	+5VS
GPIO 55	Native	PCI_GNT3#	INT PU	+3VS
GPIO 56	GPI	CLKREQ_GLAN#	EXT PD	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU (Diode)	+3VSUS
GPIO 58	GPIO	SML1_CLK	EXT PU	+3VSUS
GPIO 59	Native	NC_PU	EXT PU	+3VSUS
GPIO 60	Native	SML0ALERT#	EXT PU	+3VSUS
GPIO 61	Native	NC_TP	-	+3VSUS
GPIO 62	Native	NC_TP	-	+3VSUS
GPIO 63	Native	NC_TP	-	+3VSUS
GPIO 64	Native	NC_TP	INT TBD	+3VS
GPIO 65	Native	NC_TP	INT TBD	+3VS
GPIO 66	GPO	EDID_SELECT#	INT TBD	+3VS
GPIO 67	Native	CLK_CR48	INT TBD	+3VS
GPIO 72	GPO	PM_BATLOW#	EXT PU	+3VSUS
GPIO 73	Native	CLK_REQ0#	EXT PU	+3VSUS
GPIO 74	Native	SML1ALERT	EXT PU	+3VSUS
GPIO 75	GPIO	SML1_DATA	EXT PU	+3VSUS

EC IT8572 GPIO

EC GPIO	Use As	Signal Name
GPA0	OD	PWR_LED#
GPA1	OD	CHG_LED#
GPA2	O	CHG_FULL_LED#
GPA3	O	MUTE_LED#
GPA4	ALT	LCD_BL_PWM
GPA5	ALT	FAN_PWM
GPA6	ALT	VOLUME_LED#
GPA7	O	MEDIA_KEY_LED#
GPB0	O	BATSEL_0
GPB1	O	BATSEL_1
GPB2	O	ME_AC_PRESENT
GPB3	ALT	SMB0_CLK
GPB4	ALT	SMB0_DAT
GPB5	OD	A20GATE
GPB6	OD	RC_IN#
GPB7	O	PM_RSMRST#
GPC0		CLK_UC
GPC1	ALT	SMB1_CLK
GPC2	ALT	SMB1_DAT
GPC3	O	PM_PWRBTN#
GPC4	ALT	AC_IN_OC#
GPC5	O	OP_SD#
GPC6	ALT	BAT1_IN_OC#
GPC7	I	RFON_SW#
GPD0	I	PWRLIMIT#
GPD1	I	PM_SUSC#
GPD2	ALT	BUF_PLT_RST#
GPD3	OD	EXT_SCI#
GPD4	OD	EXT_SMI#
GPD5	O	LCD_BACKOFF#
GPD6	ALT	FAN0_TACH
GPD7	OD	EXP_GATE_LED#
GPE0	O	-
GPE1	I / PU	-
GPE2	I / PU	-
GPE3		-
GPE4	ALT	PWR_SW#
GPE5	ALT	CLK_OC#
GPE6	I	LID_SW#
GPE7	I	EXP_GATE#
GPFO	ALT	OS_LED#
GPF1	O	VSUS_ON
GPF2	I	VCCP_DV0
GPF3	I	VCCP_DV1
GPF4	ALT	TP_CLK
GPF5	ALT	TP_DAT
GPF6	O	THRO_CPU
GPF7	O	PCH_SPI_OV
PGP0	I	ME_SusPwrDnAck
PGP1	I	PM_SUSB#
PGP2		CLK_STRAPO
PGP6		CLK_STRAP1
GPH0	ALT	PM_CLKRUN#
GPH1		GFX_VR_ON
GPH2	O	CHG_EN
GPH3	O	SUSC_EC#
GPH4	O	SUSB_EC#
GPH5	OD	NUM_LED#
GPH6	OD	CAP_LED#
GPI0		HDMI_HPD
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	PCH_TEMP_ALERT#
GPI5		-
GPI6		IDLE_HPD_INT#
GPI7		-
GPJ0	O	CPU_VRON
GPJ1	O	PM_PWROK
GPJ2	ALT	VSET_EC
GPJ3	ALT	ISSET_EC
GPJ4		CPU_DV0
GPJ5	O	CPU_DV1

Design IP Source:N73JF

PCH Master		
SM-Bus Device	SM-Bus Address	
Clock Generator(ICS9LRS3197)	1101001x ( D2 )	
SO-DIMM 0	1010000x ( A0 )	
SO-DIMM 1	1010001x ( A2 )	
VID Controller(ASM8272)	0011011x ( 36 )	
EC Master (SMB1)		
SM-Bus Device	SM-Bus Address	
CPU Thermal Sensor(G781)	1001100x ( 9A )	
VGA Thermal IC(G781-1)	1001101x ( 9E )	

PCI Express		USB Port	
PCIE 1	Minicard TV Tuner	USB 0	USB Port 0
PCIE 2	Minicard WLAN	USB 1	USB Port 1
PCIE 3	Newcard	USB 2	USB Port 2
PCIE 4	USB 3.0	USB 3	USB Port 3
PCIE 5	Card Reader	USB 4	Minicard TV Tuner
PCIE 6	GLAN	USB 5	NewCard
PCIE 7		USB 6	
PCIE 8		USB 7	
		USB 8	WLAN
		USB 9	CMOS Camera
		USB 10	
		USB 11	
		USB 12	Bluetooth
		USB 13	

Device Identification		
CPU Thermal Sensor		
1st	06G023048011	G781F
2nd		
VGA Thermal Senser		
1st	06G023048010	G781-1
2nd		
Clock Gen		
1st	06G011614010	ICS9LVS3161
2nd		



## FDI disable: (For discrete graphic)

1. NC:  
FDI\_TX# [0:7], FDI\_TX [0:7], VCC\_AXGSENSE, VSS\_AXGSENSE
2. Pull-down to GND via  $1K\Omega \pm 5\%$  resistor:  
FDI\_FSYNC [0:1], FDI\_LSYNC [0:1], FDI\_INT, GFX\_IMON  
~15mW power saving
3. Connected to GND:  
VCCAXG
4. Can be connected to GND directly:  
DPLL\_REF\_CLK, DPLL\_REF\_CLK#
5. Connect to +V1.05S rail:  
VCCFDIPLL

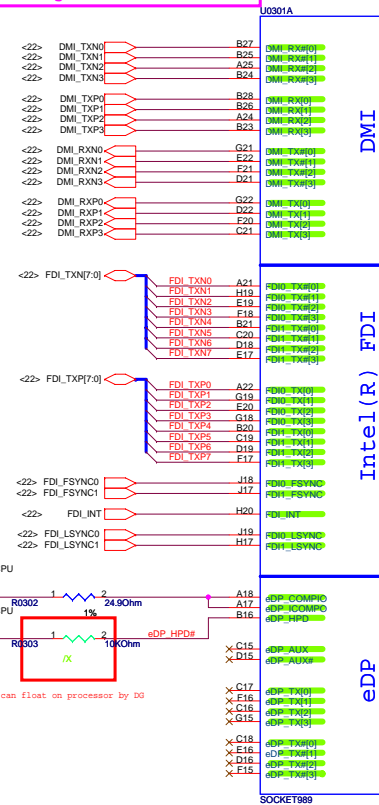
## eDP disable/Enable

CFG[4]:

Enable: Mount R0503, R0303=1K

Disable: un-mount R0503, R0303=10Kohm

## CPU socket P/N change to 12G011909893



DMI

Intel(R) FDI

eDP

SOCKET989

PCI EXPRESS\* - GRAPHICS

MISC

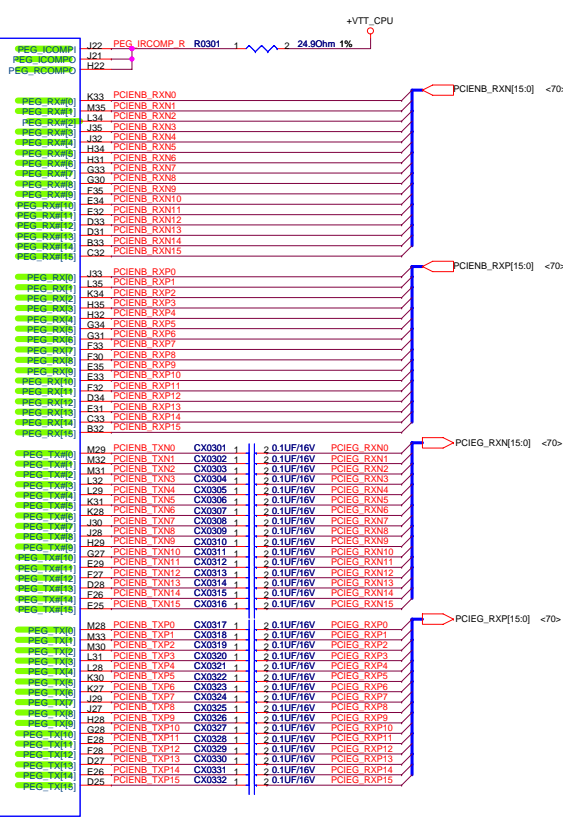
THERMAL

PWR MANAGEMENT

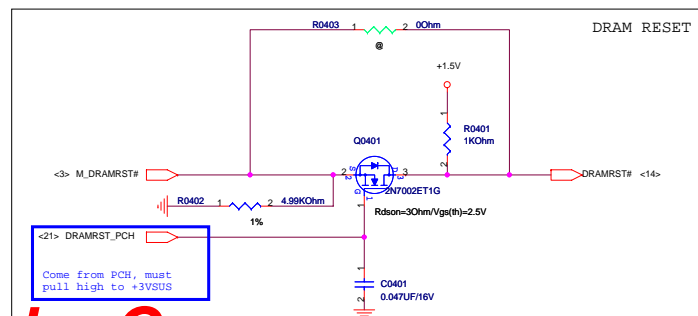
CLOCKS

DDR3

JTAG &amp; BPM

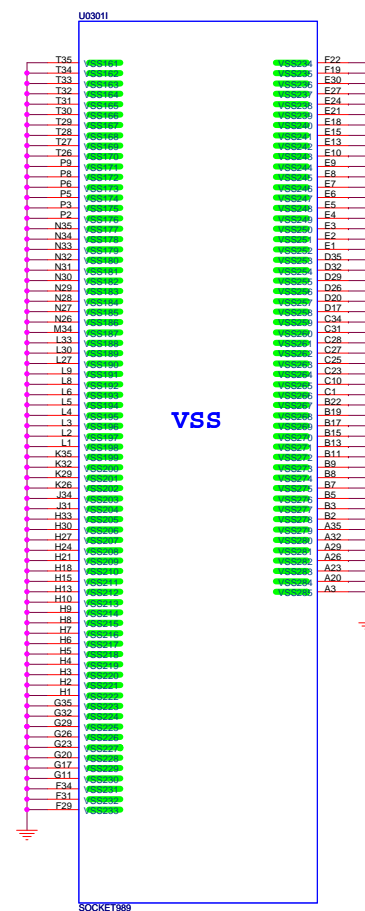
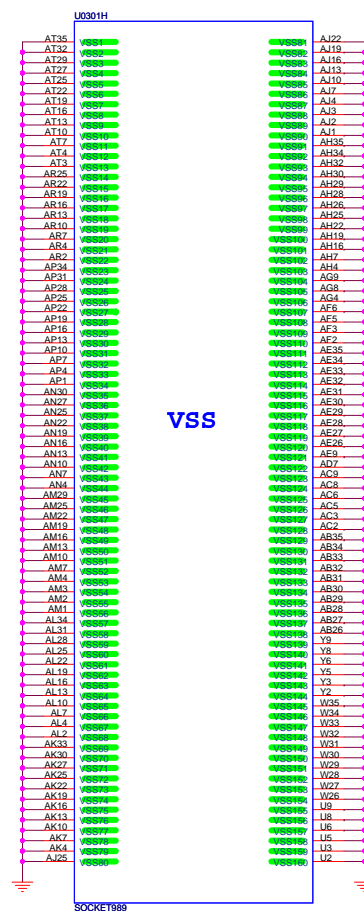
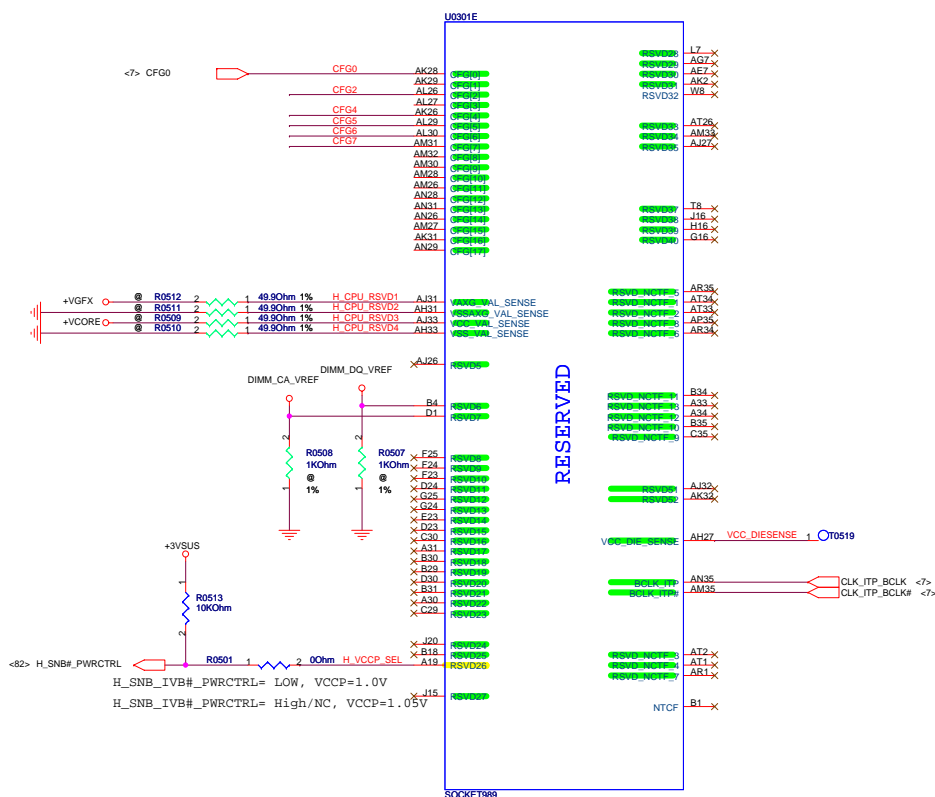








1, 拿掉測點, 以需有Via 2, 拿掉net  
CFG1, CFG3, CFG8~CFG17, 以防止layout后處理一直報錯。



**CFG strapping information:**

## CFG[2]: PEG Static Lane Reversal (For the 16X)

- 1: (Default) Normal Operation; Lane # definition matches socket pin map definition
- 0: Lane Reversed

#### CFG[4]: Display Port Presence Strap

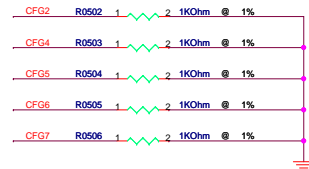
- 1 : (Default) Disable; No Physical Display Port attached to Embedded Display Port
- 0 : Enable; An external Display Port device is connected to the Embedded Display port

**CFG[6:5]: PCIE Port Bifurcation Straps**

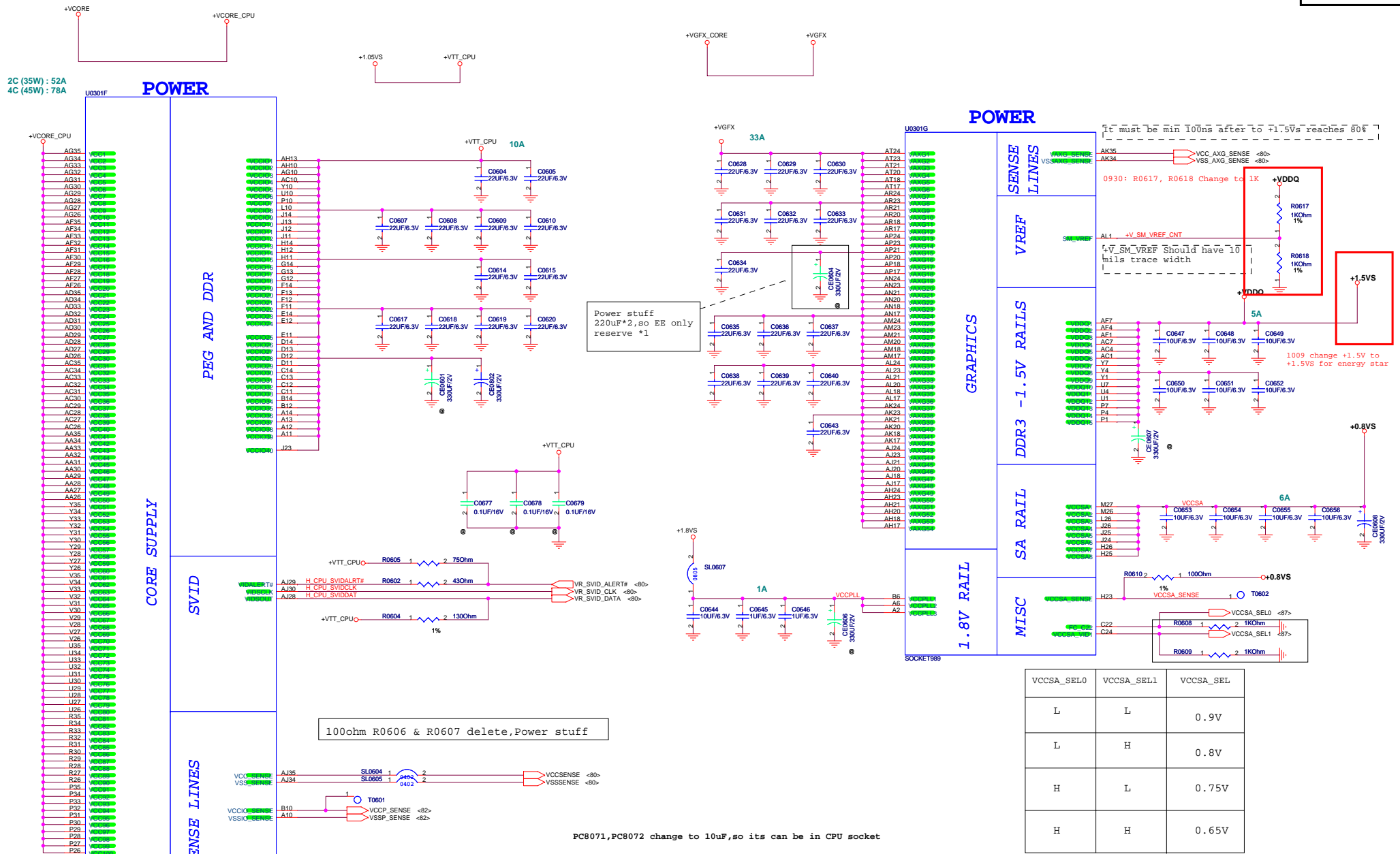
- 11 : (Default) X16 - Device 1 functions 1 and 2 disable
- 10 : X8, X8 - Device 1 function 1 enabled; Function 2 disable
- 01 : Reserved - (Device 1 Function 1 disable ; Function 2 enable)
- 00 : X8, X4 X4 - Device 1 function 1 and 2 enabled

### CFG[7]: Defer Training

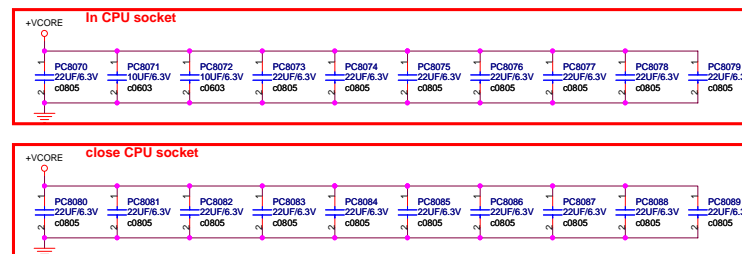
- 1: (Default) PEG Train immediately following xxRESETB de assertion
- 0: PEG Wait for BIOS for training



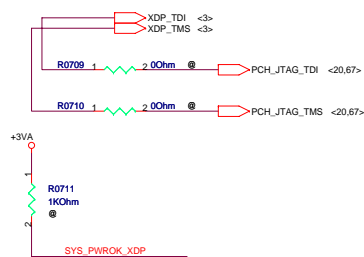
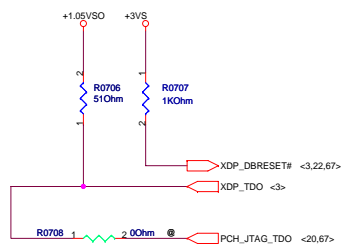
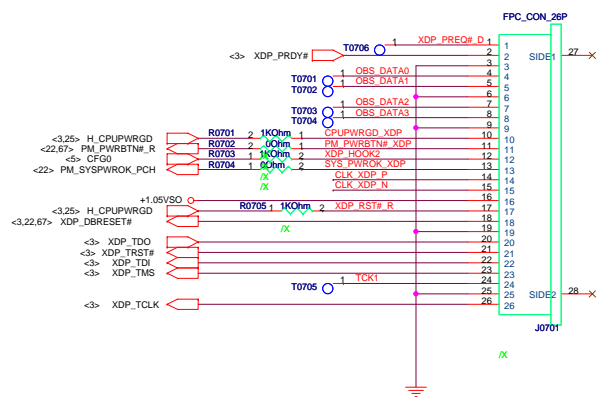




VCCSA_SEL0	VCCSA_SEL1	VCCSA_SEL
L	L	0.9V
L	H	0.8V
H	L	0.75V
H	H	0.65V














	5	4	3	2	1
D					D
C					C
B					B
A					A
	5	4	3	2	1

		<b>Title :</b> NB_****	
ASUSTeK COMPUTER INC. NB3		<b>Engineer:</b> <i>Wish</i>	
Size A	Project Name N73Sv		Rev 1.0
Date: <u>Wednesday, October 13, 2010</u>		Sheet <u>9</u> of <u>95</u>	




	5	4	3	2	1
D					D
C					C
B					B
A					A
<div>ASUS®</div> <div>Title : NB_****</div>					
ASUSTeK COMPUTER INC. NB3 Engineer: Wish					
Size	Project Name				Rev
A	N73Sv				1.0
Date: Wednesday, October 13, 2010				Sheet	10 of 95

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	5	4	3	2	1
D					D
C					C
B					B
A					A
	5	4	3	2	1

		<b>Title :</b> NB_****	
ASUSTeK COMPUTER INC. NB3		<b>Engineer:</b> <i>Wish</i>	
Size A	Project Name N73Sv		Rev 1.0
Date: <u>Wednesday, October 13, 2010</u>		Sheet <u>11</u> of <u>95</u>	



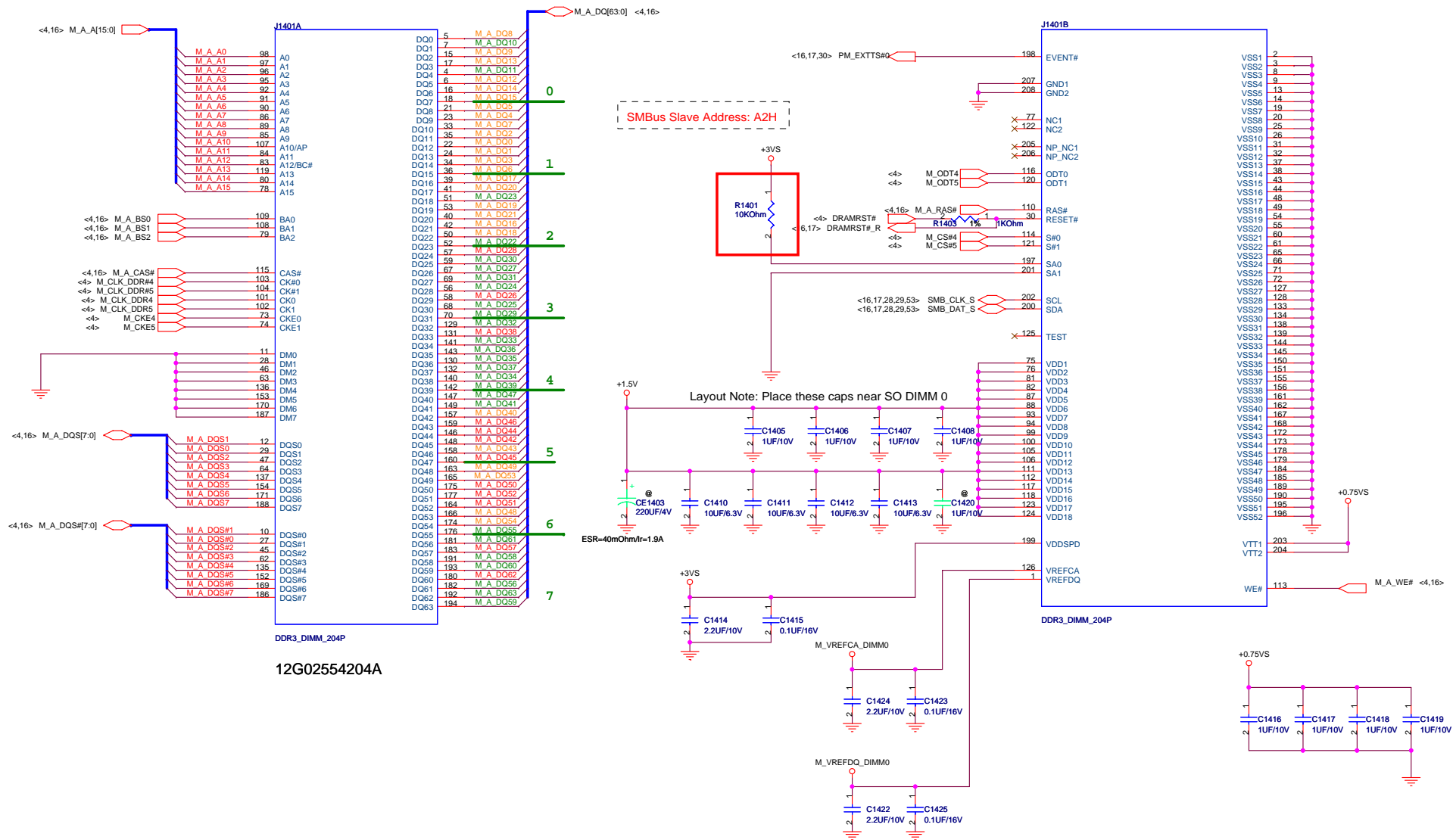








# CH-A-4mm-TOP









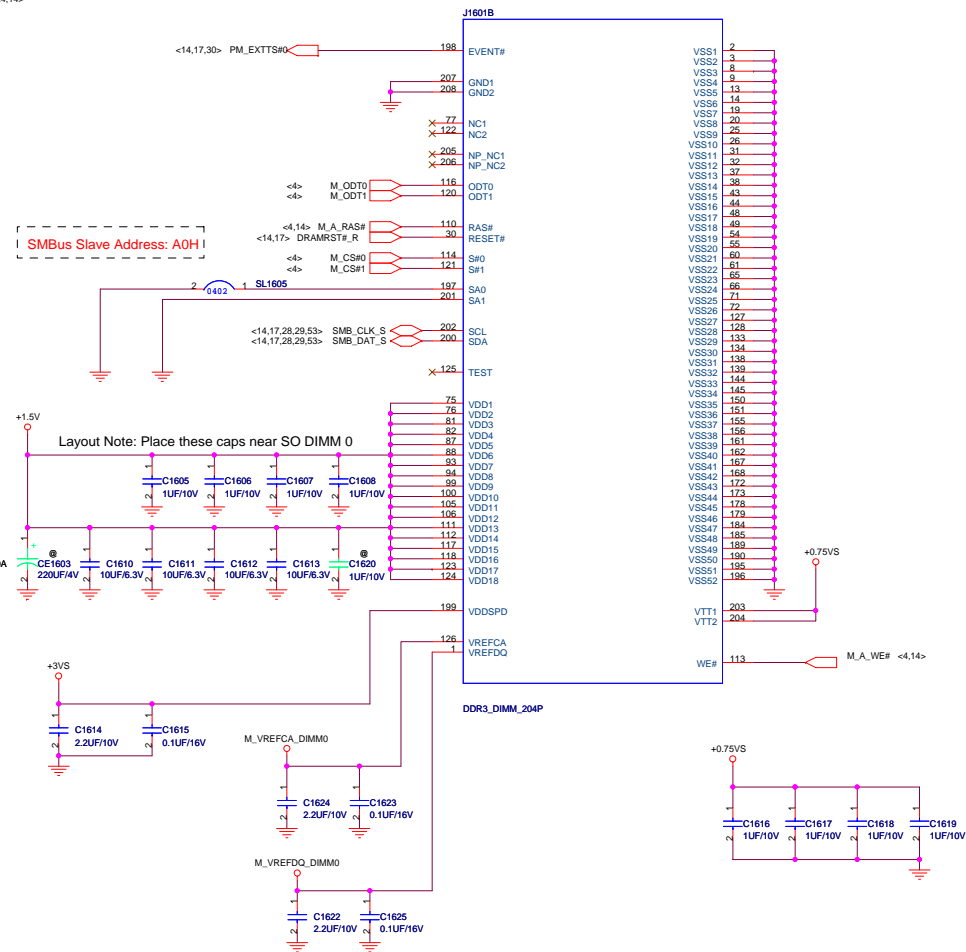
**H601A**

**Pinout:**

- Address Lines (A0-A15):**
  - M\_A A0: 98, A0
  - M\_A A1: 97, A1
  - M\_A A2: 96, A2
  - M\_A A3: 95, A3
  - M\_A A4: 92, A4
  - M\_A A5: 91, A5
  - M\_A A6: 90, A6
  - M\_A A7: 86, A7
  - M\_A A8: 89, A8
  - M\_A A9: 85, A9
  - M\_A A10: 107, A10
  - M\_A A11: 84, A11
  - M\_A A12: 83, A12
  - M\_A A13: 119, A13
  - M\_A A14: 80, A14
  - M\_A A15: 78, A15
- Data Lines (DQ0-DQ31):**
  - DQ0: 5, M\_A DQ0
  - DQ1: 15, M\_A DQ1
  - DQ2: 17, M\_A DQ2
  - DQ3: 15, M\_A DQ3
  - DQ4: 6, M\_A DQ4
  - DQ5: 16, M\_A DQ5
  - DQ6: 18, M\_A DQ6
  - DQ7: 21, M\_A DQ7
  - DQ8: 23, M\_A DQ8
  - DQ9: 33, M\_A DQ9
  - DQ10: 35, M\_A DQ10
  - DQ11: 22, M\_A DQ11
  - DQ12: 34, M\_A DQ12
  - DQ13: 24, M\_A DQ13
  - DQ14: 34, M\_A DQ14
  - DQ15: 36, M\_A DQ15
  - DQ16: 39, M\_A DQ16
  - DQ17: 41, M\_A DQ17
  - DQ18: 51, M\_A DQ18
  - DQ19: 53, M\_A DQ19
  - DQ20: 40, M\_A DQ20
  - DQ21: 42, M\_A DQ21
  - DQ22: 50, M\_A DQ22
  - DQ23: 52, M\_A DQ23
  - DQ24: 57, M\_A DQ24
  - DQ25: 59, M\_A DQ25
  - DQ26: 67, M\_A DQ26
  - DQ27: 69, M\_A DQ27
  - DQ28: 56, M\_A DQ28
  - DQ29: 58, M\_A DQ29
  - DQ30: 68, M\_A DQ30
  - DQ31: 70, M\_A DQ31
  - DQ32: 129, M\_A DQ32
  - DQ33: 131, M\_A DQ33
  - DQ34: 141, M\_A DQ34
  - DQ35: 143, M\_A DQ35
  - DQ36: 132, M\_A DQ36
  - DQ37: 140, M\_A DQ37
  - DQ38: 140, M\_A DQ38
  - DQ39: 147, M\_A DQ39
  - DQ40: 149, M\_A DQ40
  - DQ41: 149, M\_A DQ41
  - DQ42: 157, M\_A DQ42
  - DQ43: 159, M\_A DQ43
  - DQ44: 146, M\_A DQ44
  - DQ45: 158, M\_A DQ45
  - DQ46: 160, M\_A DQ46
  - DQ47: 160, M\_A DQ47
  - DQ48: 163, M\_A DQ48
  - DQ49: 165, M\_A DQ49
  - DQ50: 173, M\_A DQ50
  - DQ51: 177, M\_A DQ51
  - DQ52: 164, M\_A DQ52
  - DQ53: 174, M\_A DQ53
  - DQ54: 176, M\_A DQ54
  - DQ55: 181, M\_A DQ55
  - DQ56: 183, M\_A DQ56
  - DQ57: 191, M\_A DQ57
  - DQ58: 193, M\_A DQ58
  - DQ59: 193, M\_A DQ59
  - DQ60: 180, M\_A DQ60
  - DQ61: 182, M\_A DQ61
  - DQ62: 192, M\_A DQ62
  - DQ63: 194, M\_A DQ63
- Control Lines:**
  - CAS#: 115, CAS#
  - RAS#: 103, RAS#
  - WE#: 104, WE#
  - CS#: 101, CS#
  - B0: 102, B0
  - B1: 72, B1
  - B2: 74, B2
  - B3: 73, B3
  - B4: 72, B4
  - B5: 72, B5
  - B6: 72, B6
  - B7: 72, B7
  - B8: 72, B8
  - B9: 72, B9
  - B10: 72, B10
  - B11: 72, B11
  - B12: 72, B12
  - B13: 72, B13
  - B14: 72, B14
  - B15: 72, B15

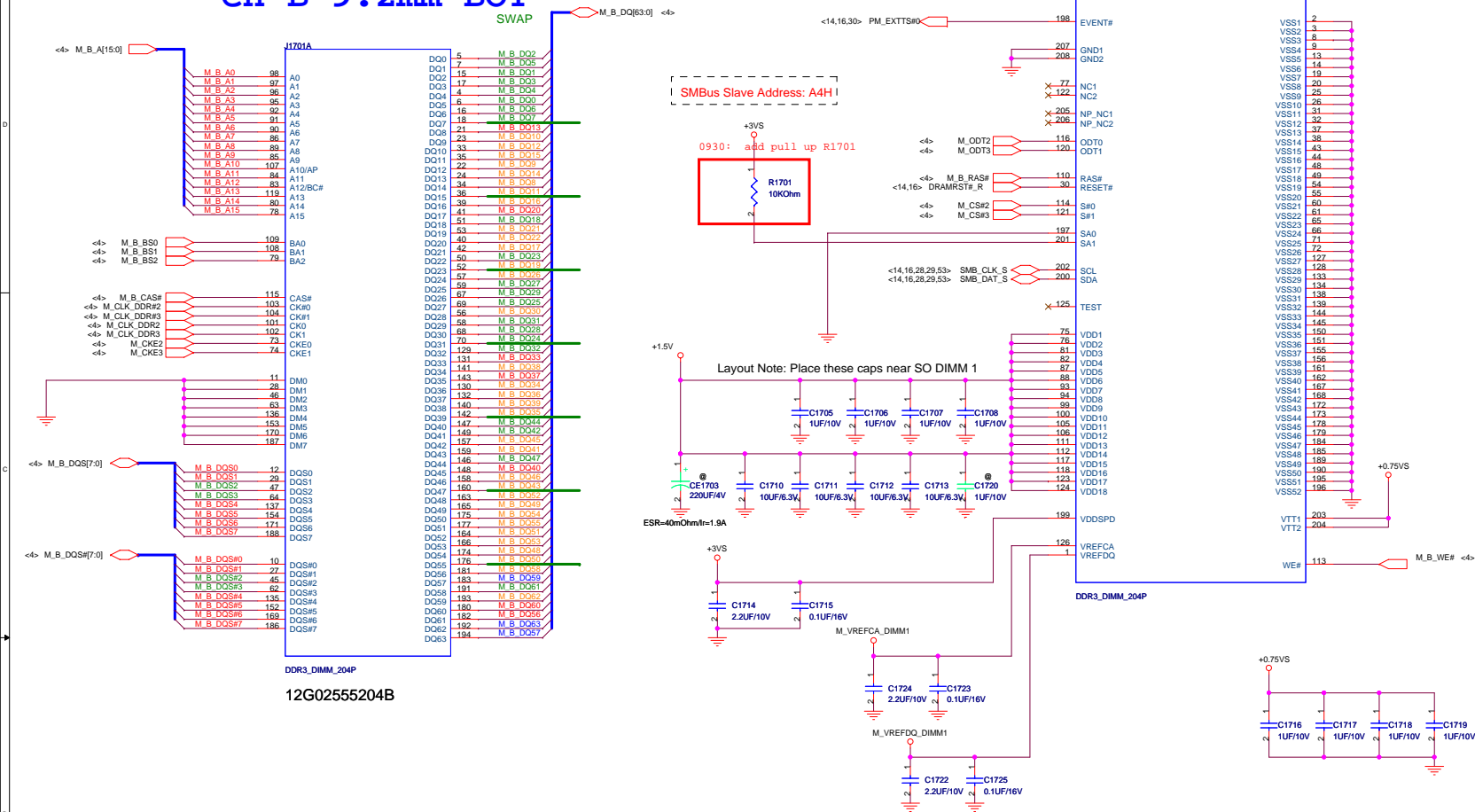
**ESR=40mOhm/1=1.9A**

**DDR3 DIMM 204P**

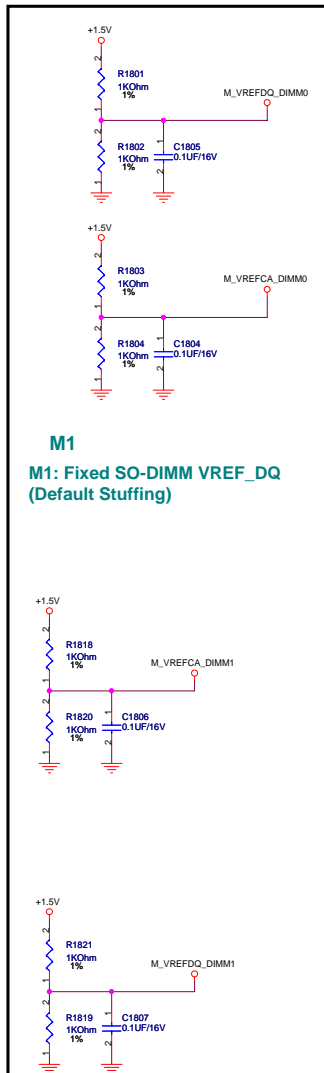




## CH-B-9.2mm-BOT







For DDR3\_VREF command & address.



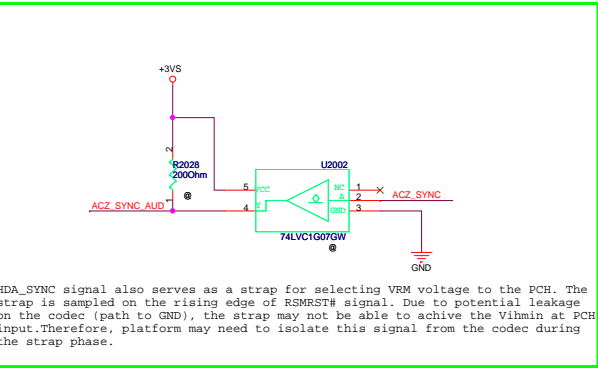
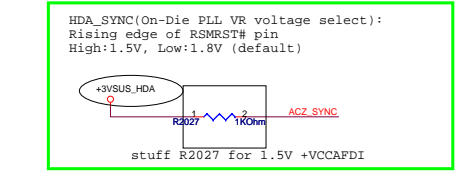




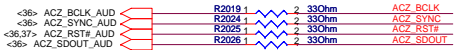
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Clear CMOS	Shunt
Keep CMOS	Open (Default)

TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

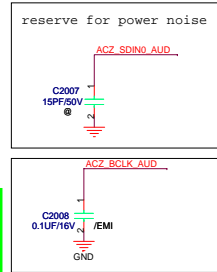


### HD Audio



GPIO33 is a signal used for Flash  
Descriptor security Override/ME debug mode  
HFI : D0, D1, LOW Enable

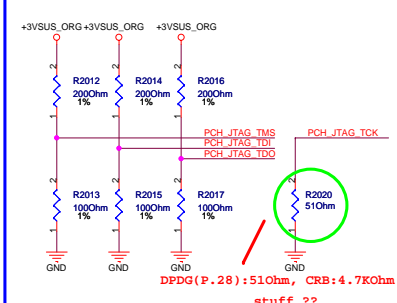
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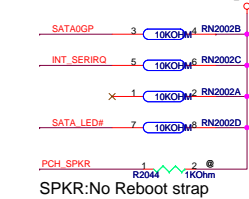
ACZ\_SDOUT:(1) PCH: Internal PD 20k  
ohm, VIL=0.35V, VIH=0.65~3.3V (2)  
ALC269:VIL<0.35\*3.3V, VIH>0.65\*3.3V  
0930: Maunt for ME firmware update



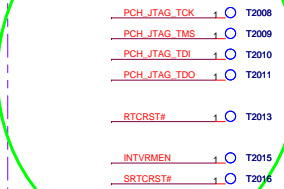
### JTAG



### For PU/PD

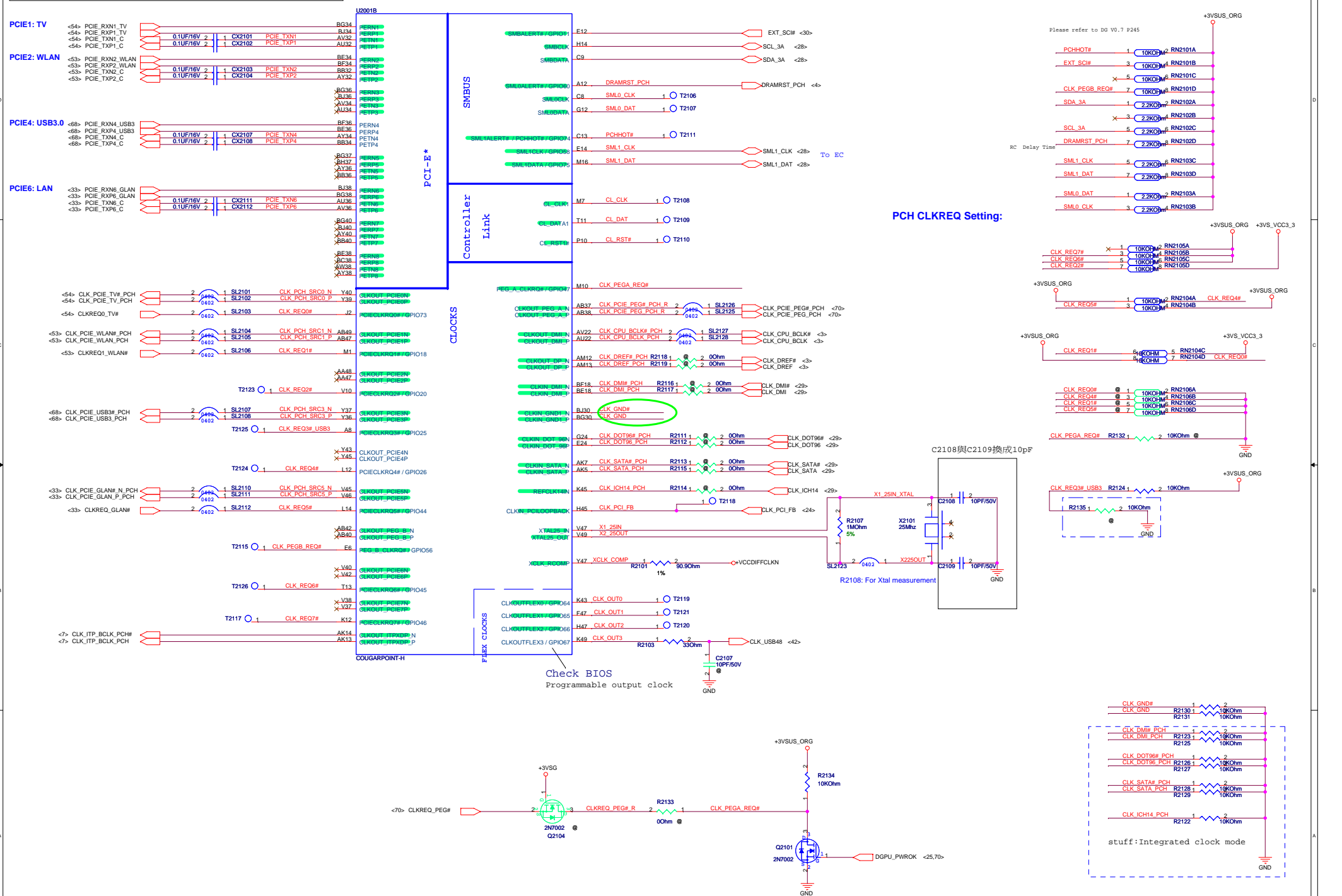


### Boundary Scan TP (PCH)





If support PCIE 3.0, pls change all 0.1uF to 0.22uF





















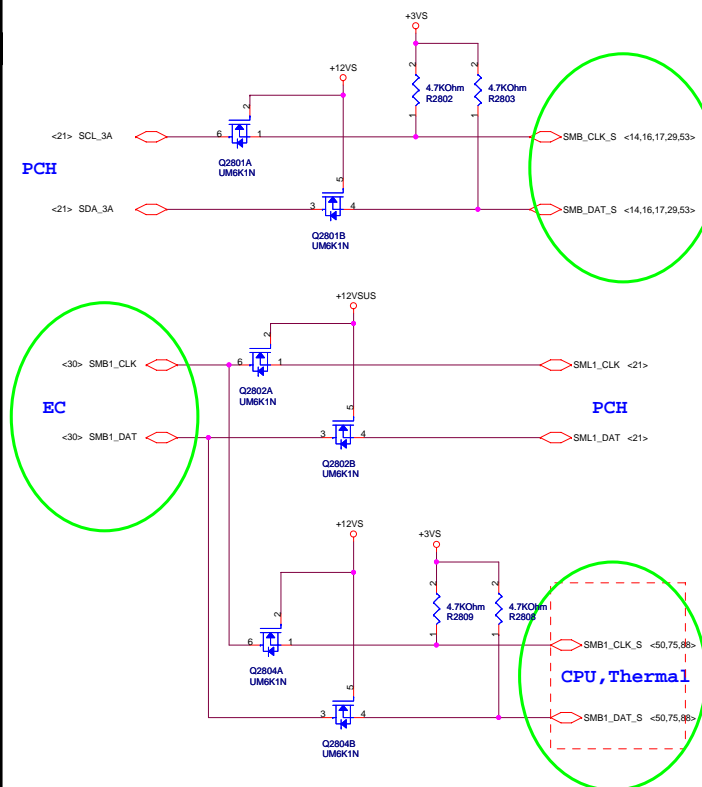
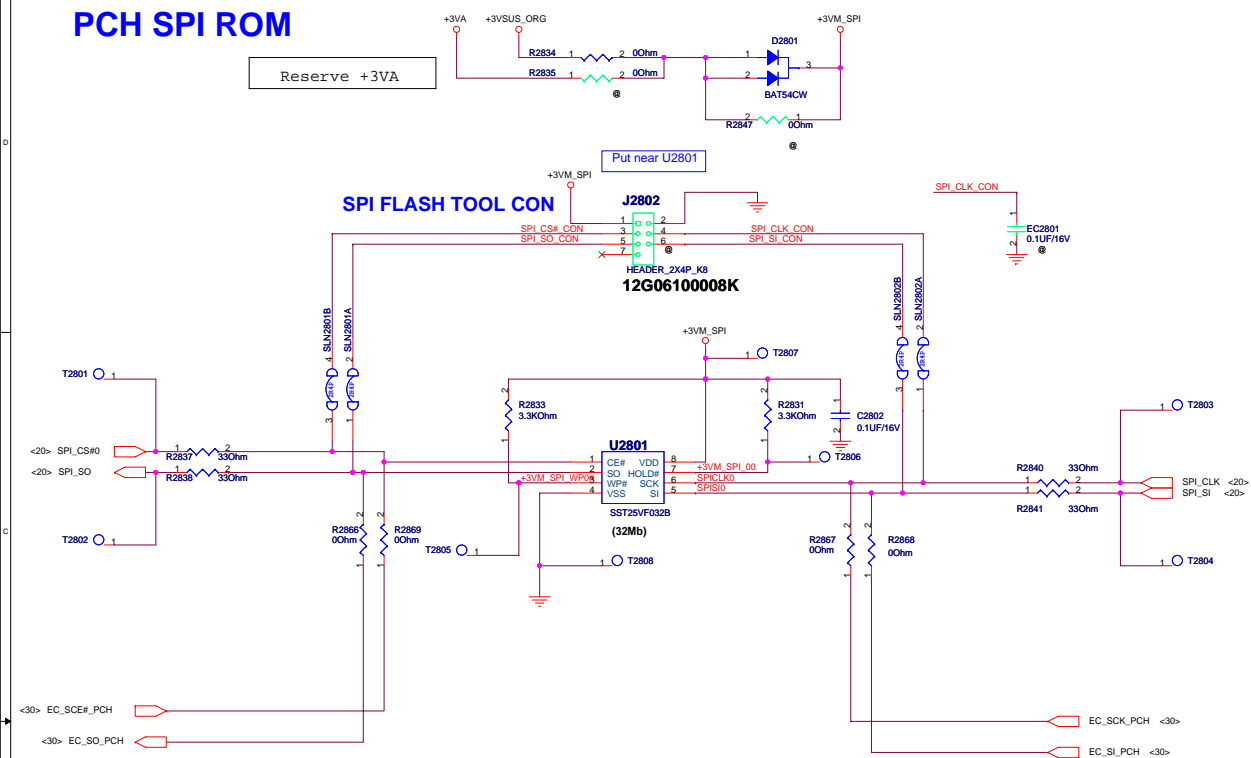








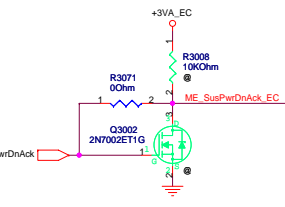
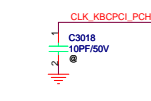
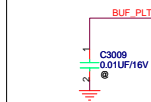
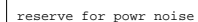
## PCH SPI ROM



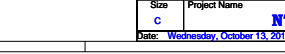
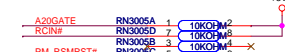
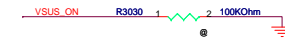
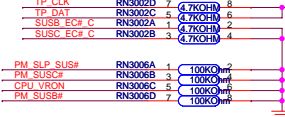
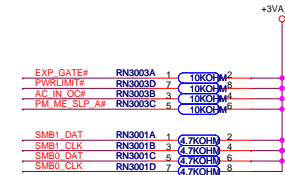
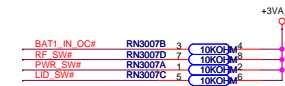
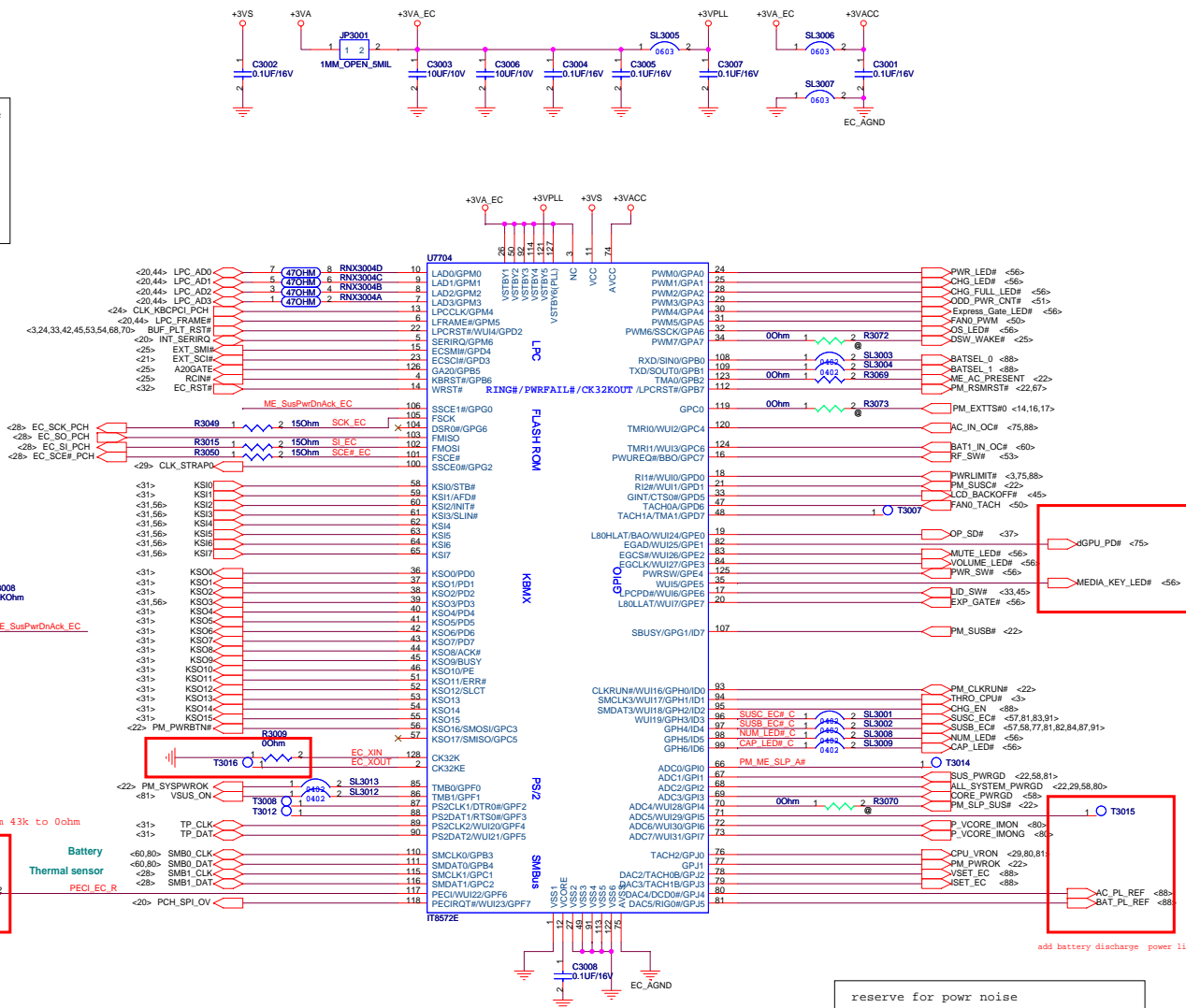
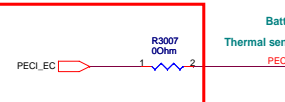






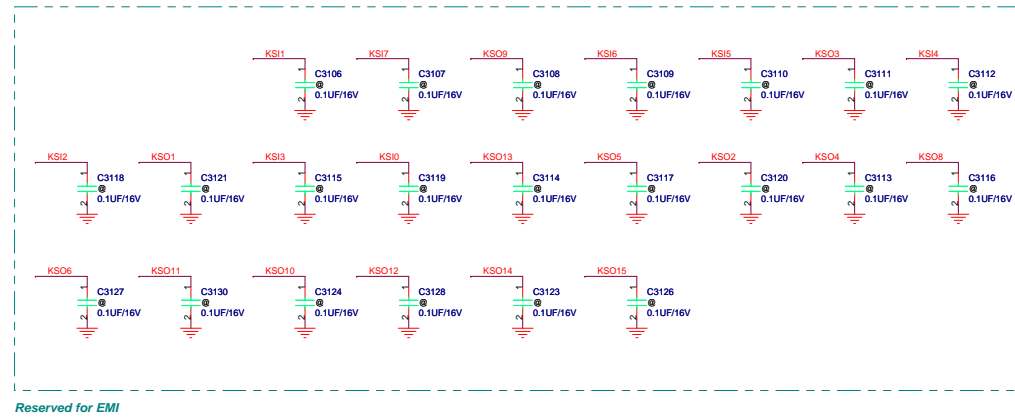
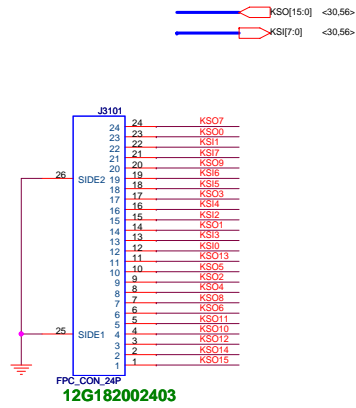


FOR ITE Suggestion, Change R3007 form 43k to 0ohm

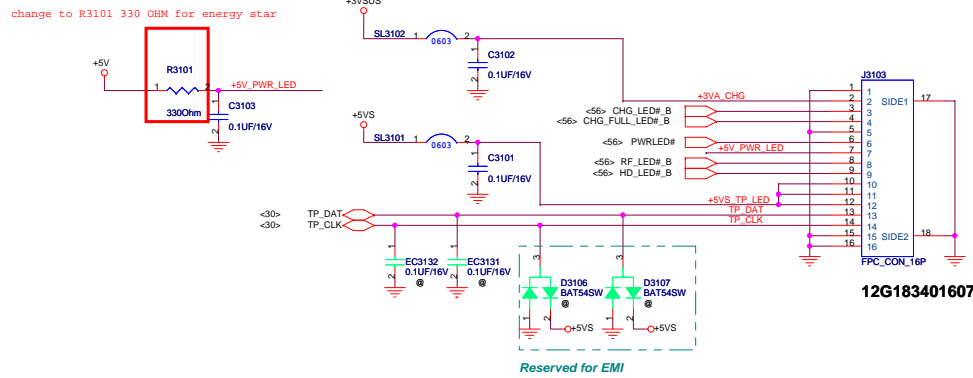




## Keyboard Connector

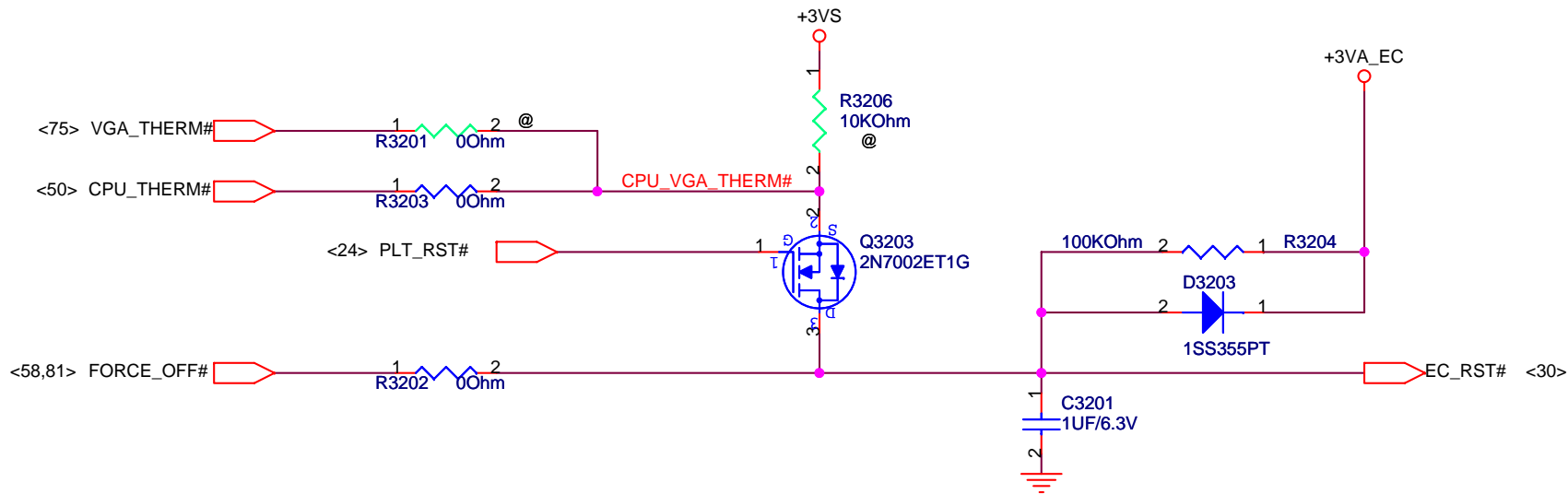


## TouchPad Connector



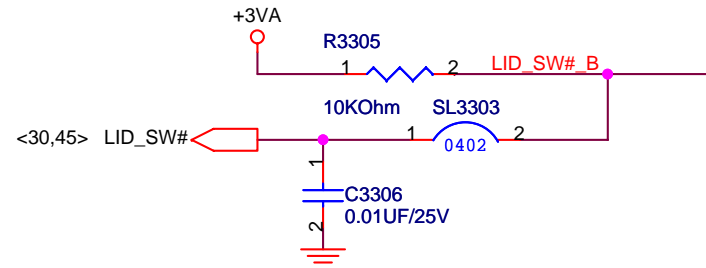
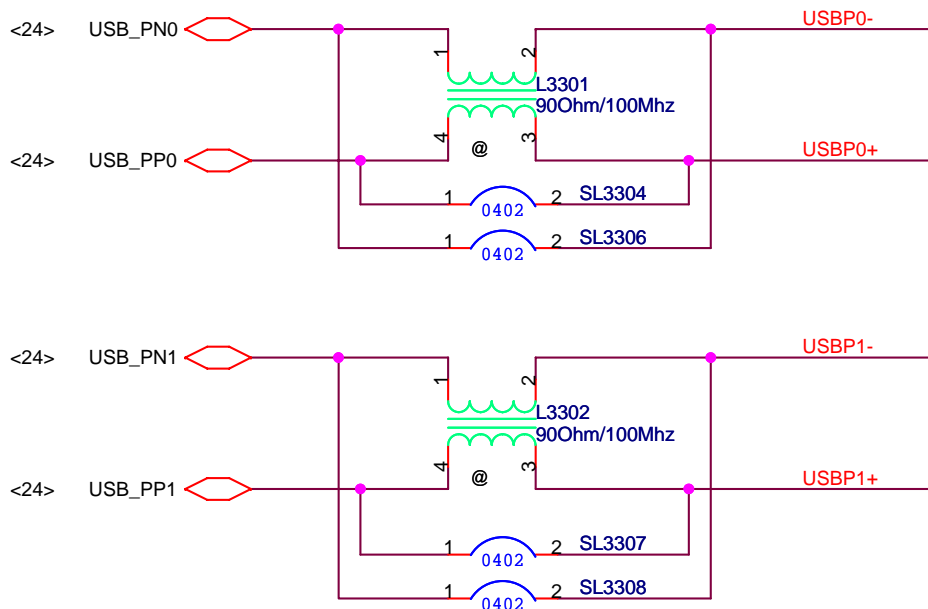
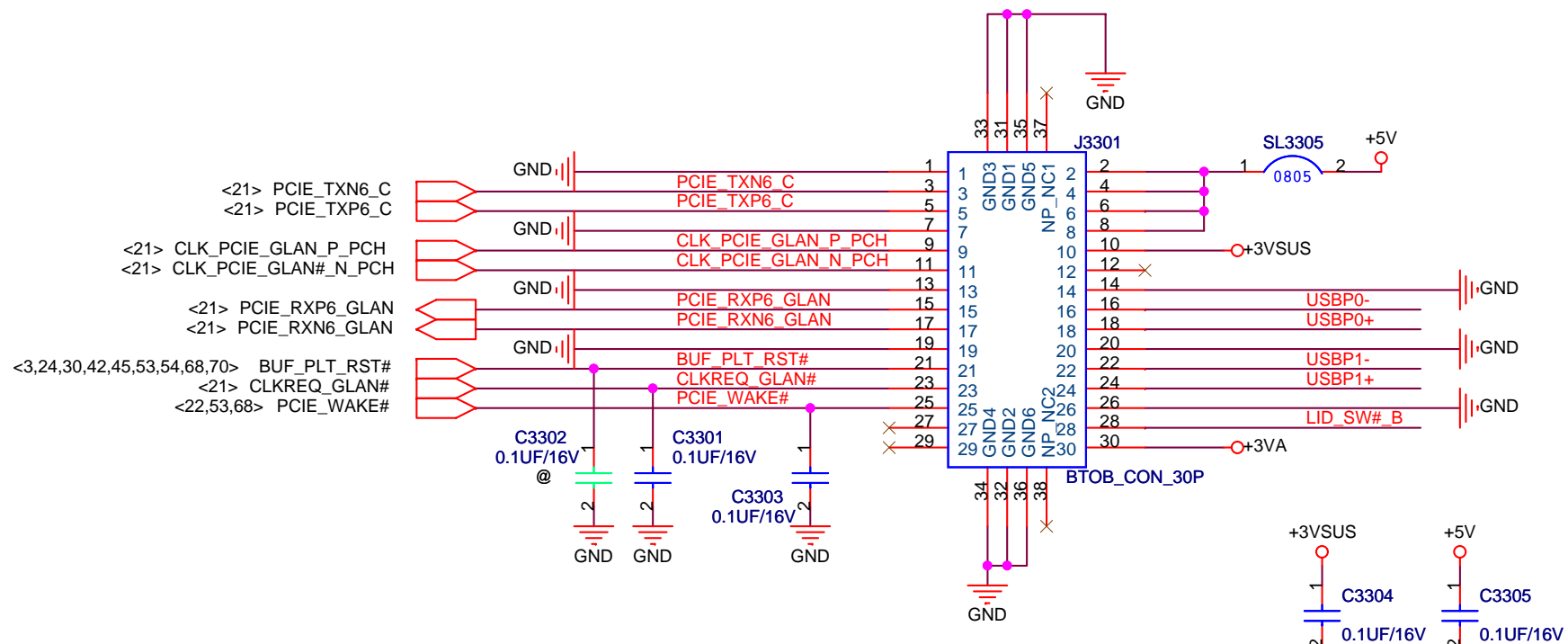


# Main Board



<b>ASUS</b>		<b>Title :</b> RST_Reset Circuit	
ASUSTeK COMPUTER INC. NB3		<b>Engineer:</b> Wish	
Size A	Project Name N73Sv		Rev 1.0
Date: Wednesday, October 13, 2010		Sheet	32 of 95





Title : LAN\_AR8131

ASUSTeK COMPUTER INC. NB3

Engineer: Wish

Size  
A

Project Name

N73Sv

Rev  
1.0

Date: Wednesday, October 13, 2010

Sheet 33 of 95





Title : LAN\_RJ45 Conn.

ASUSTeK COMPUTER INC. NB3Engineer: Wish

Size B	Project Name N73Sv	Rev 1.0
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Date: Wednesday, October 13, 2010Sheet 34 of 95

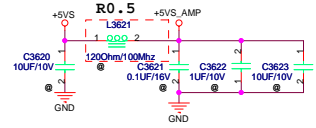


Date: Wednesday, October 18, 2018

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# DIGITAL



## Digital

<37.38> EAPD  
<38> SPDIF1\_OUT

Internal pull high 50K

PC-BEEP

269\_VA : 02G611005006  
269\_VB : 02G611005010

ALC269Q-VBS-GR

SENSE A

FRONT L

FRONT R

MIC2 INT L

MIC2 INT R

T3629

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

GND

GND\_AUDIO

For EMI

SL3651 0603

GND

GND\_AUDIO

1.5V

C3634 100PF/50V

C3635 0.1UF/16V

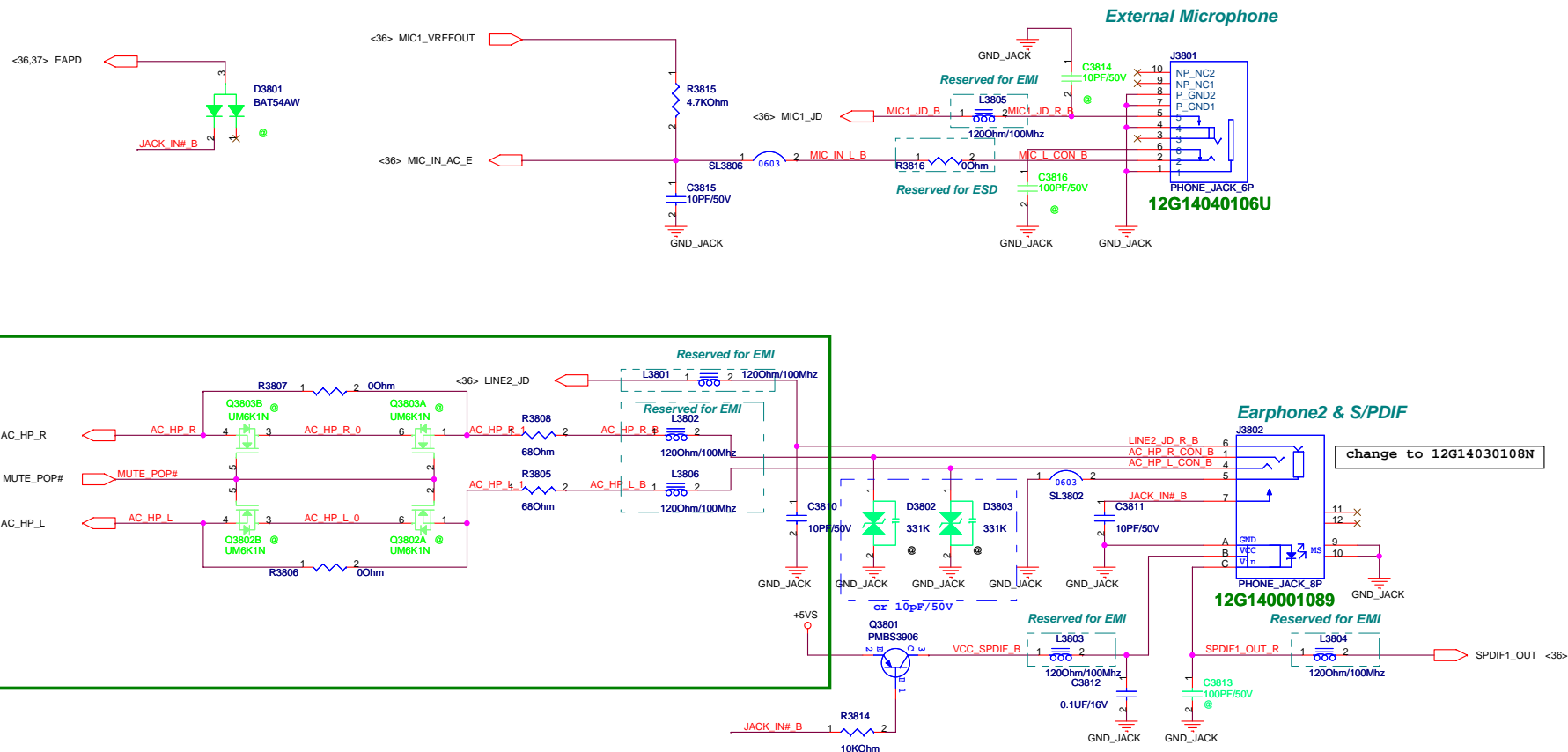
GND



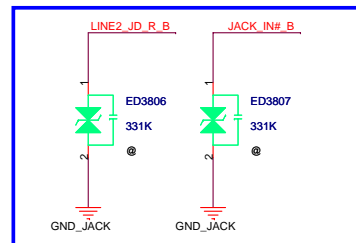




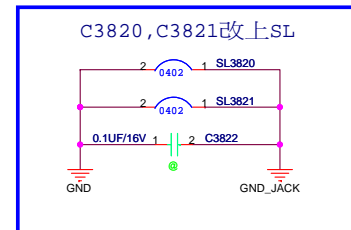
# AUDIO



## For EMI Reserve




## For EMI Reserve



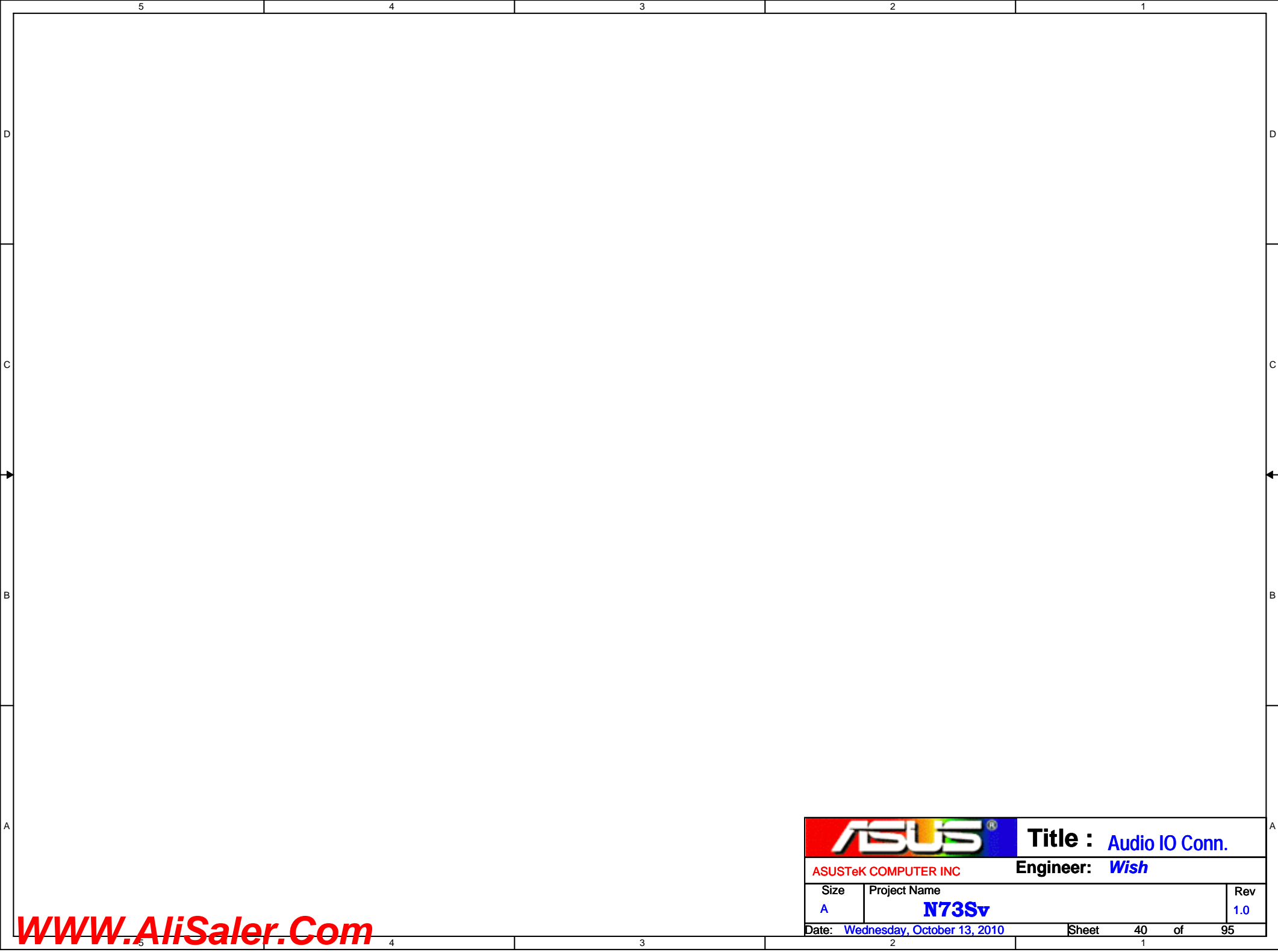
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ASUSTek COMPUTER INC. NB2		Engineer: Wish			
Size	Project Name			Rev	
Custom	N738v			1.0	
Date: Wednesday, October 13, 2010		Sheet	38	of	95



	5	4	3	2	1
D					D
C					C
B					B
A					A
	5	4	3	2	1

		<b>Title :</b> AUD_****	
ASUSTeK COMPUTER INC. NB3		<b>Engineer:</b> Wish	
Size A	Project Name N73Sv		Rev 1.0
Date: Wednesday, October 13, 2010		Sheet 39	of 95





		<b>Title :</b> Audio IO Conn.	
ASUSTeK COMPUTER INC		<b>Engineer:</b> Wish	
Size A	Project Name N73Sv		Rev 1.0
Date: Wednesday, October 13, 2010		Sheet	40 of 95





**Title :** Audio IO Conn.

ASUSTeK COMPUTER INC

Engineer: *Wish*

Size

A

Project Name
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**N73Sv**

Rev
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1.0

Date: Wednesday, October 13, 2010

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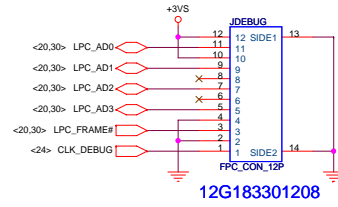








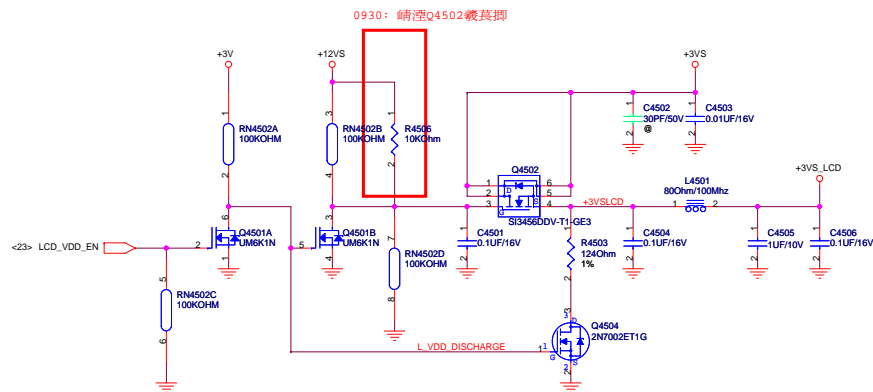
LPC Debug Port



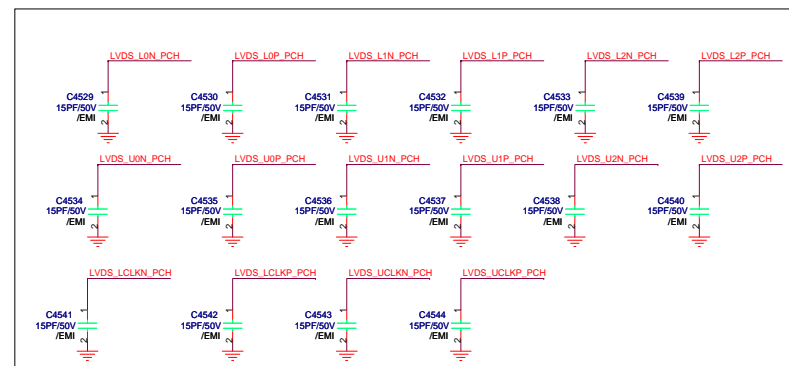
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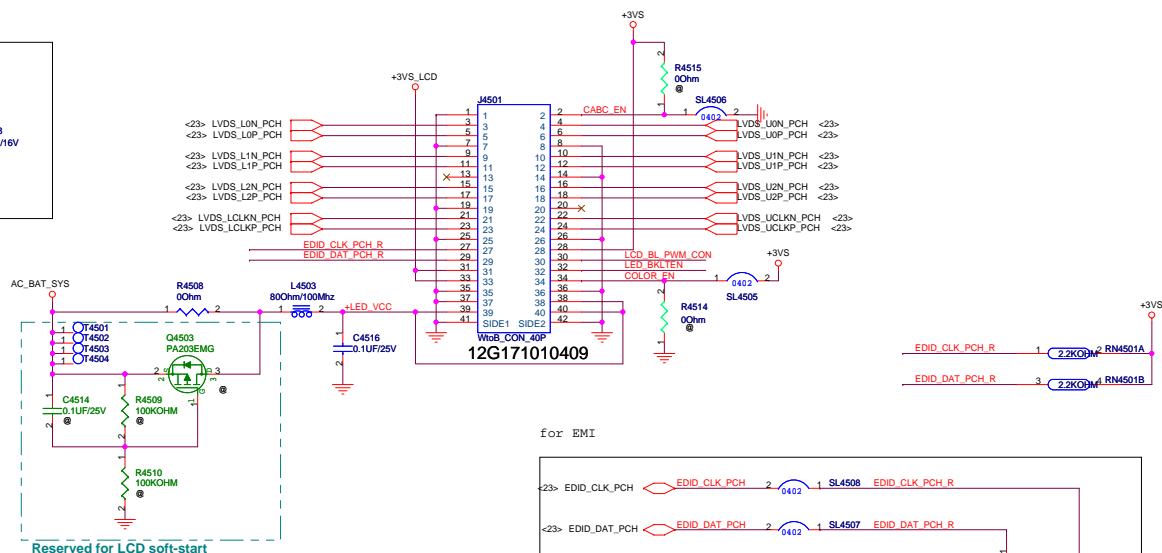
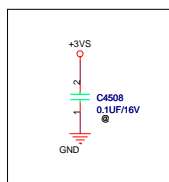
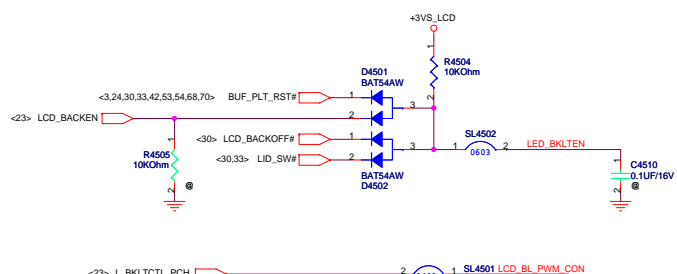
## LCD Power



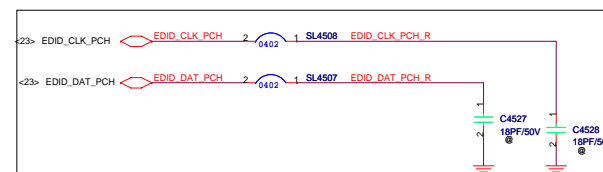
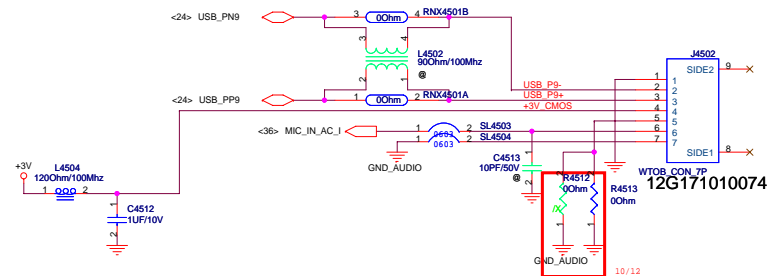
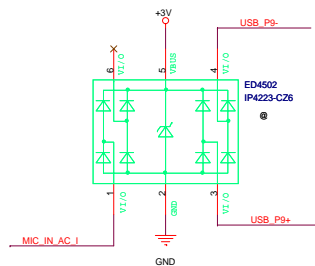
for EMI



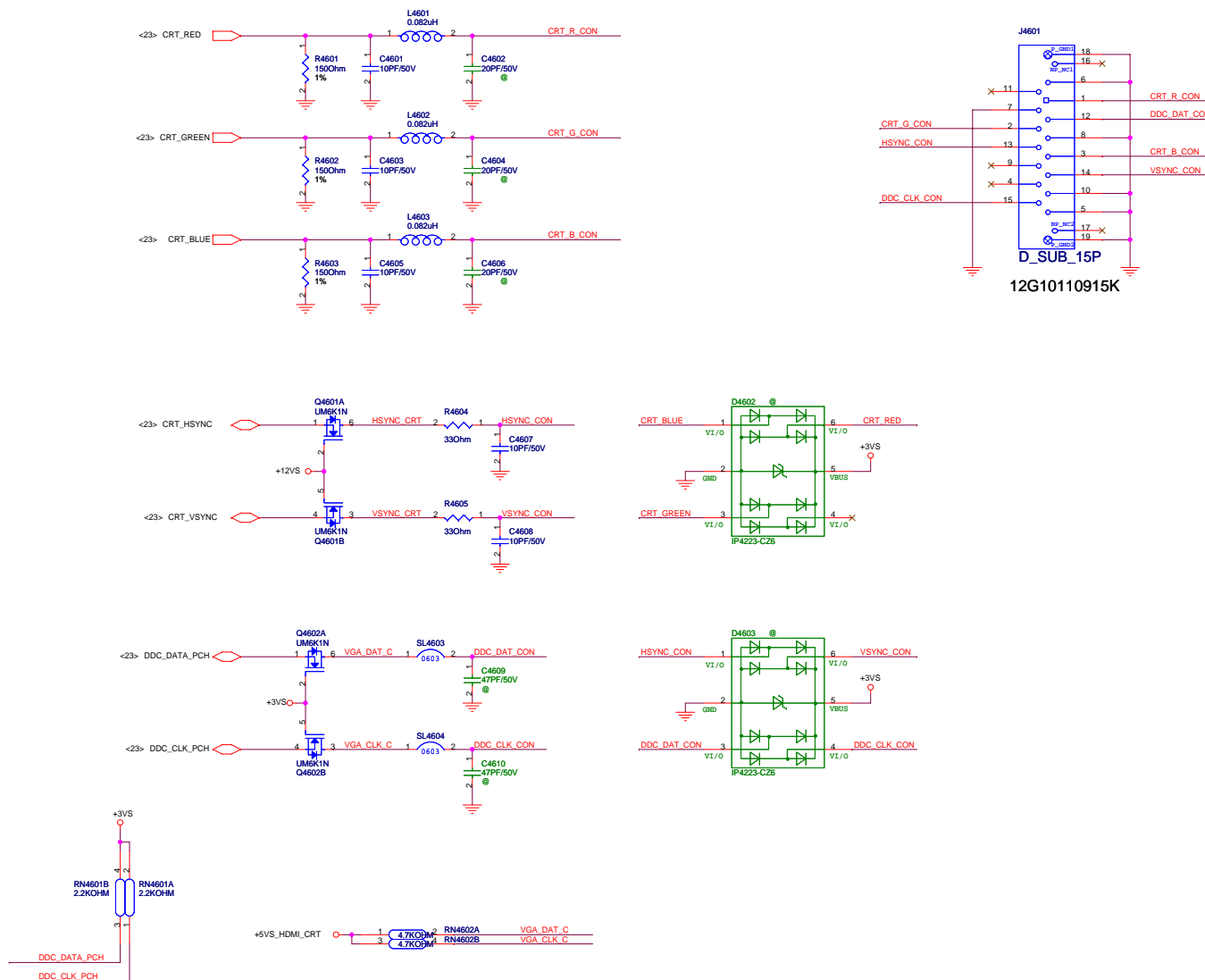
## Panel Connector



for EMI

**CMOS & Int. Mic.**

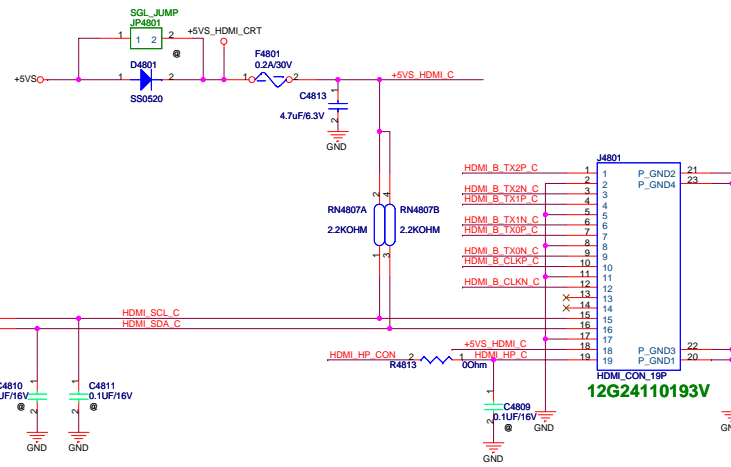
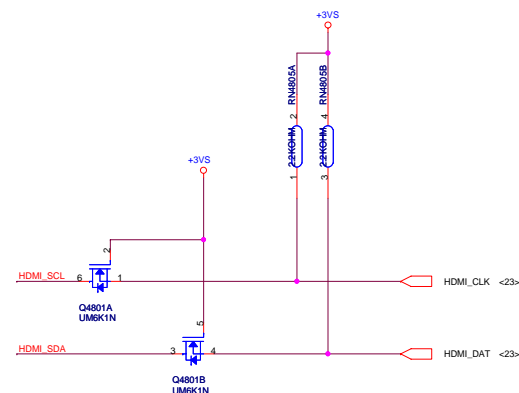
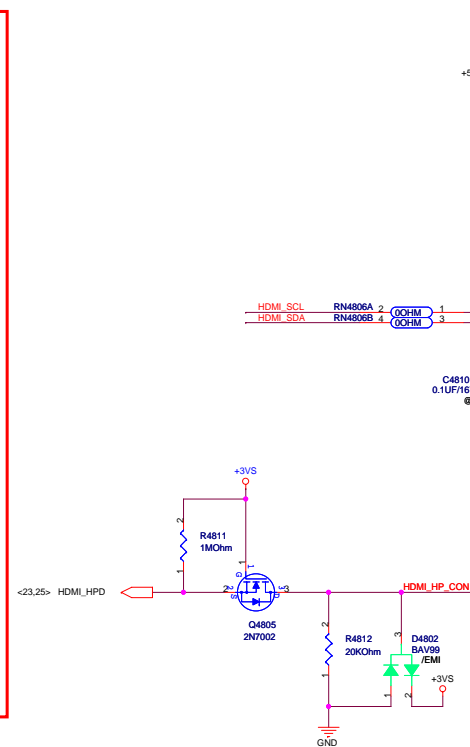
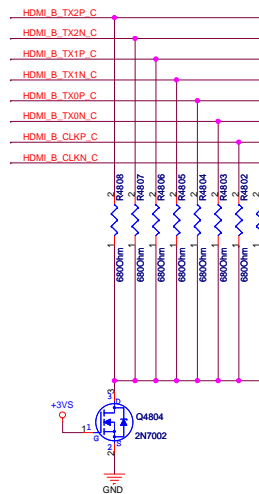
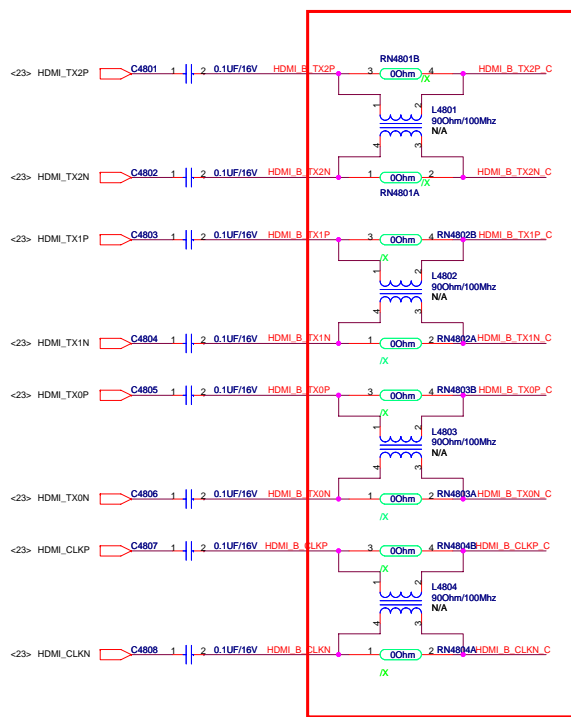




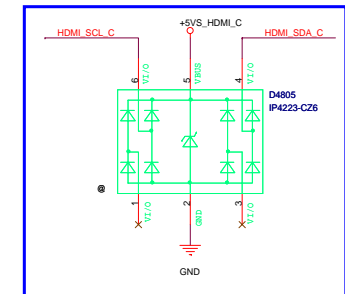
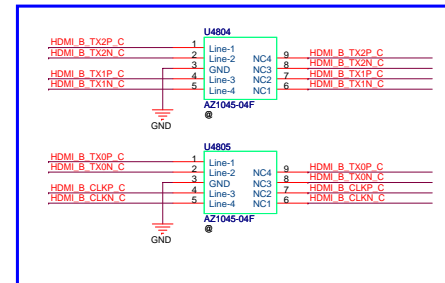








Keep R4809/R4810 = 100K/10K and mount D4802 in case of HPD input is 5V or 3.3V and chip has internal pull down resistor.



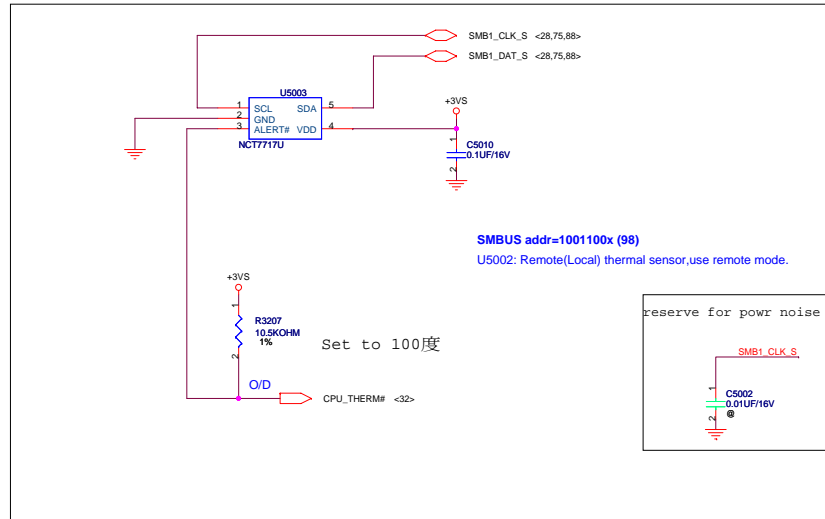






## CPU Thermal Sensor

change Thermal sensor solution



Route CPU\_THRM\_DA , CPU\_THRM\_DC and on the same layer

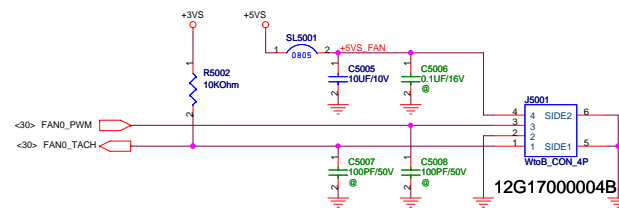
```

-----OTHER SIGNALS
10 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
10 mils
-----OTHER SIGNALS

```

**Avoid FSB,Power**

## DC FAN Control



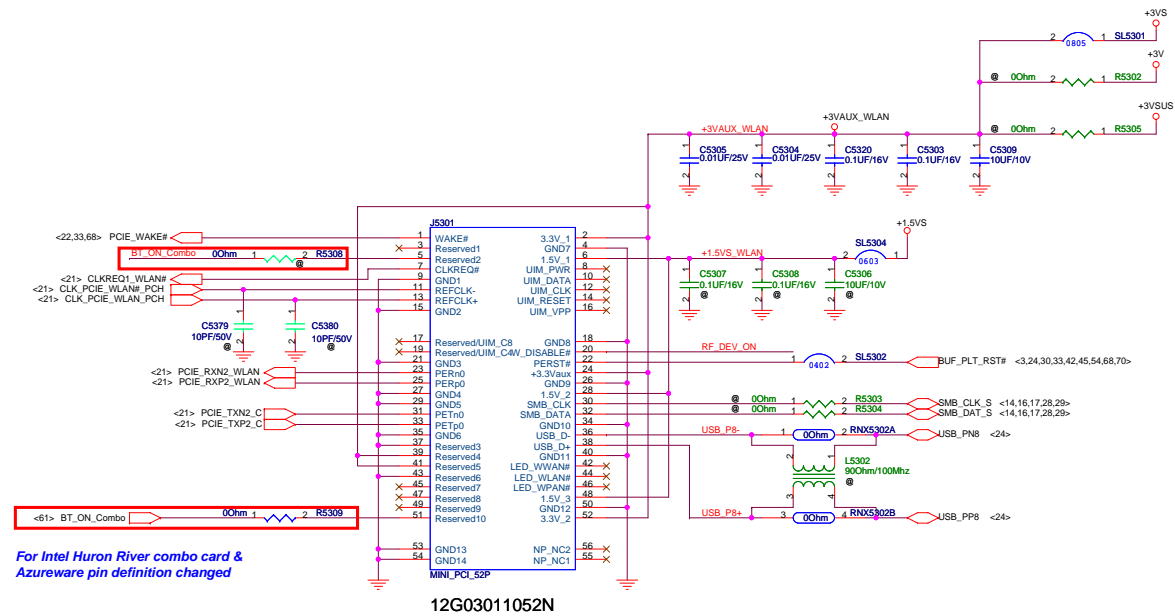




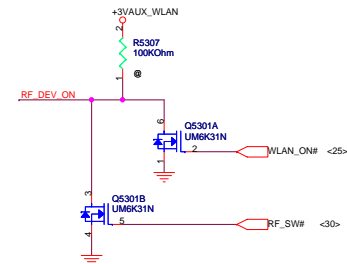
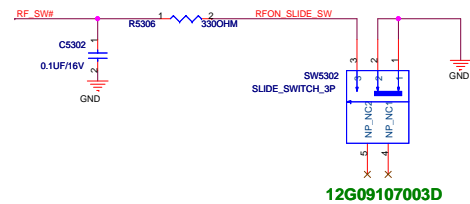




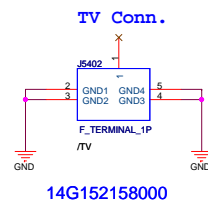
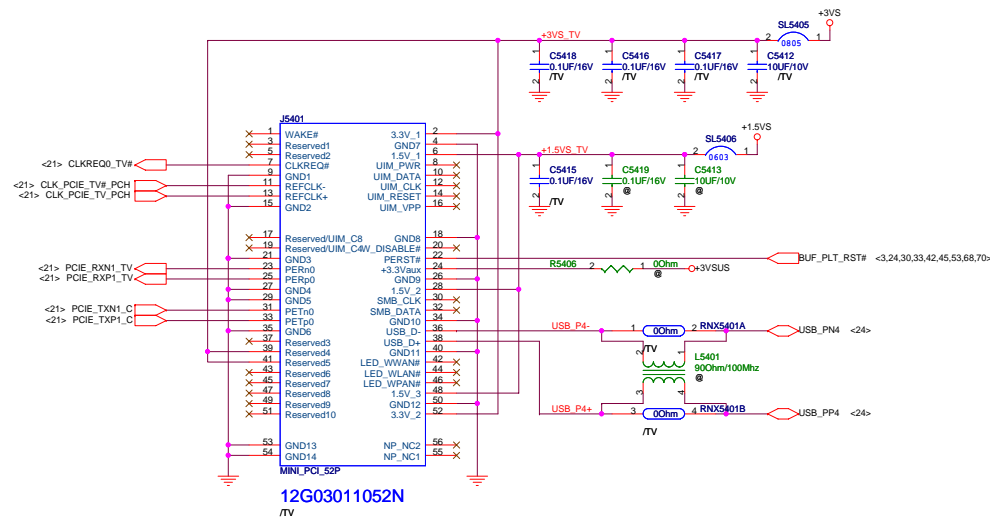




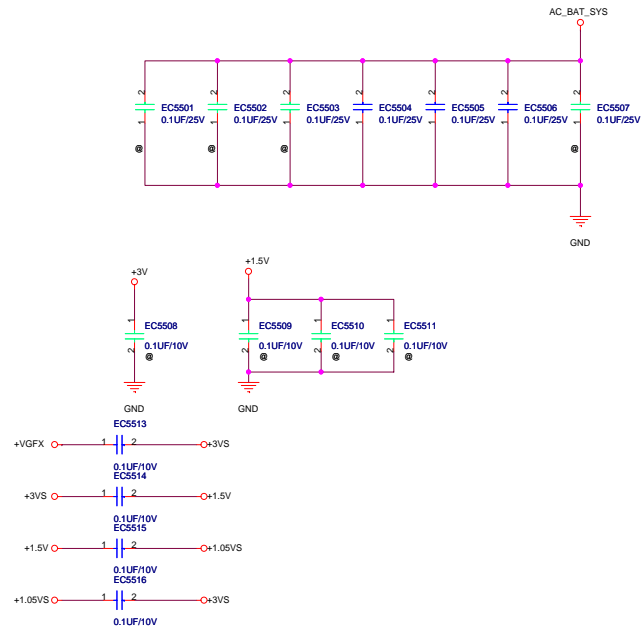
## RF SWITCH







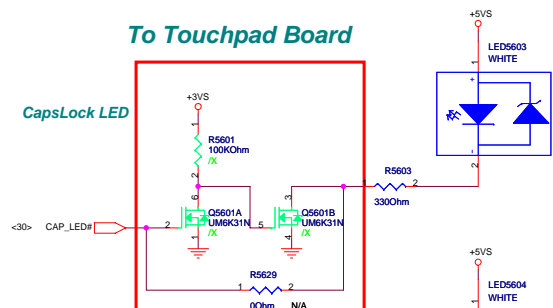




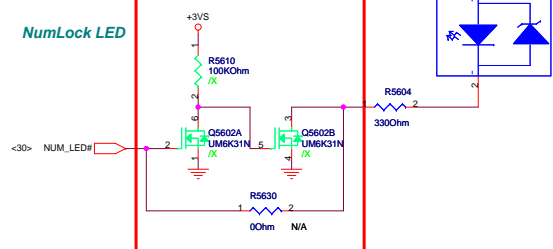


## To Touchpad Board

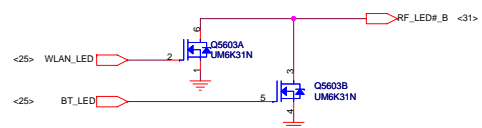
## CapsLock LED



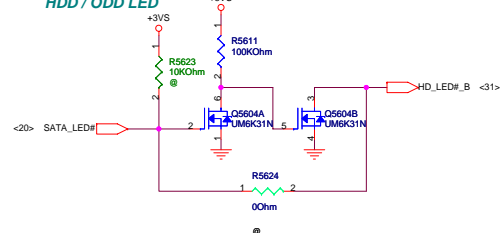
## NumLock LED



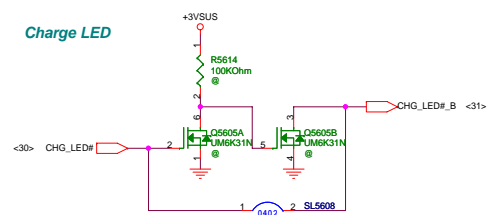
## Wireless ON LED



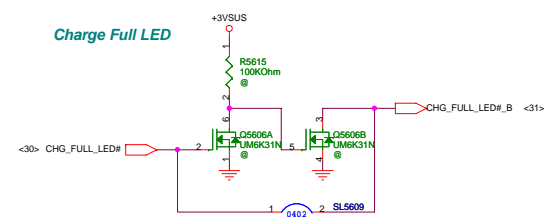
## HDD / ODD LED



## Charge LED

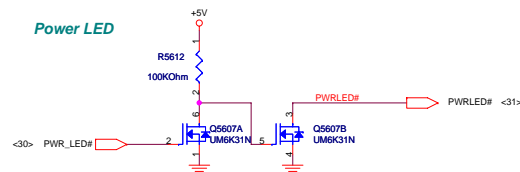


## Charge Full LED

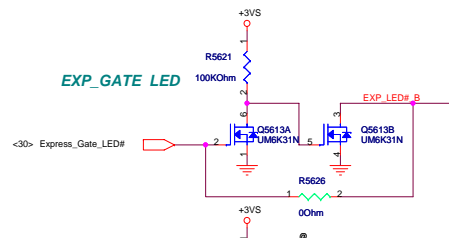


delete dGPU/IGPU LED

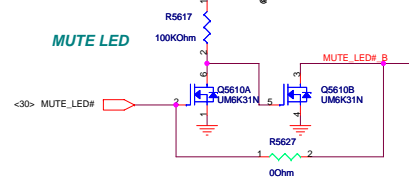
## Power LED



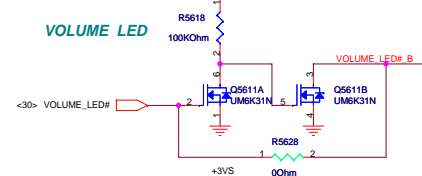
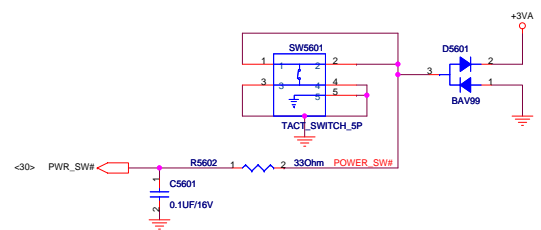
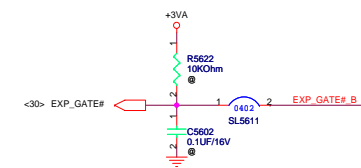
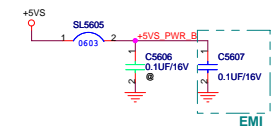
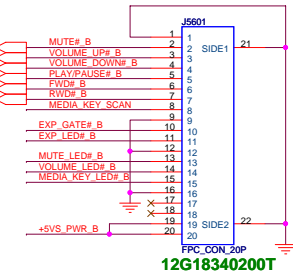
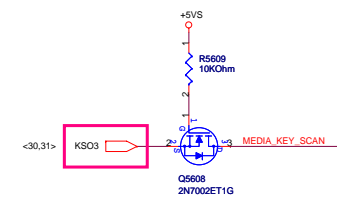
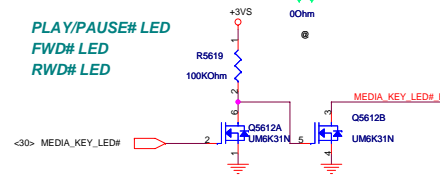
## EXP\_GATE LED



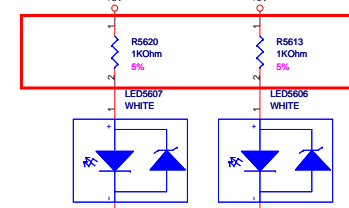
## MUTE LED



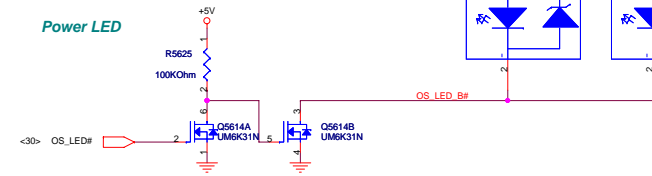
## VOLUME LED

PLAY/PAUSE# LED  
FWD# LED  
RWD# LED

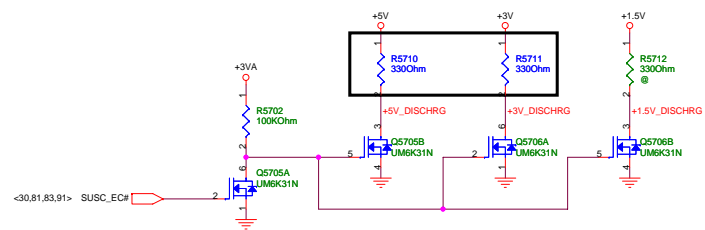
change R5620 R5613 to 1k for energy star



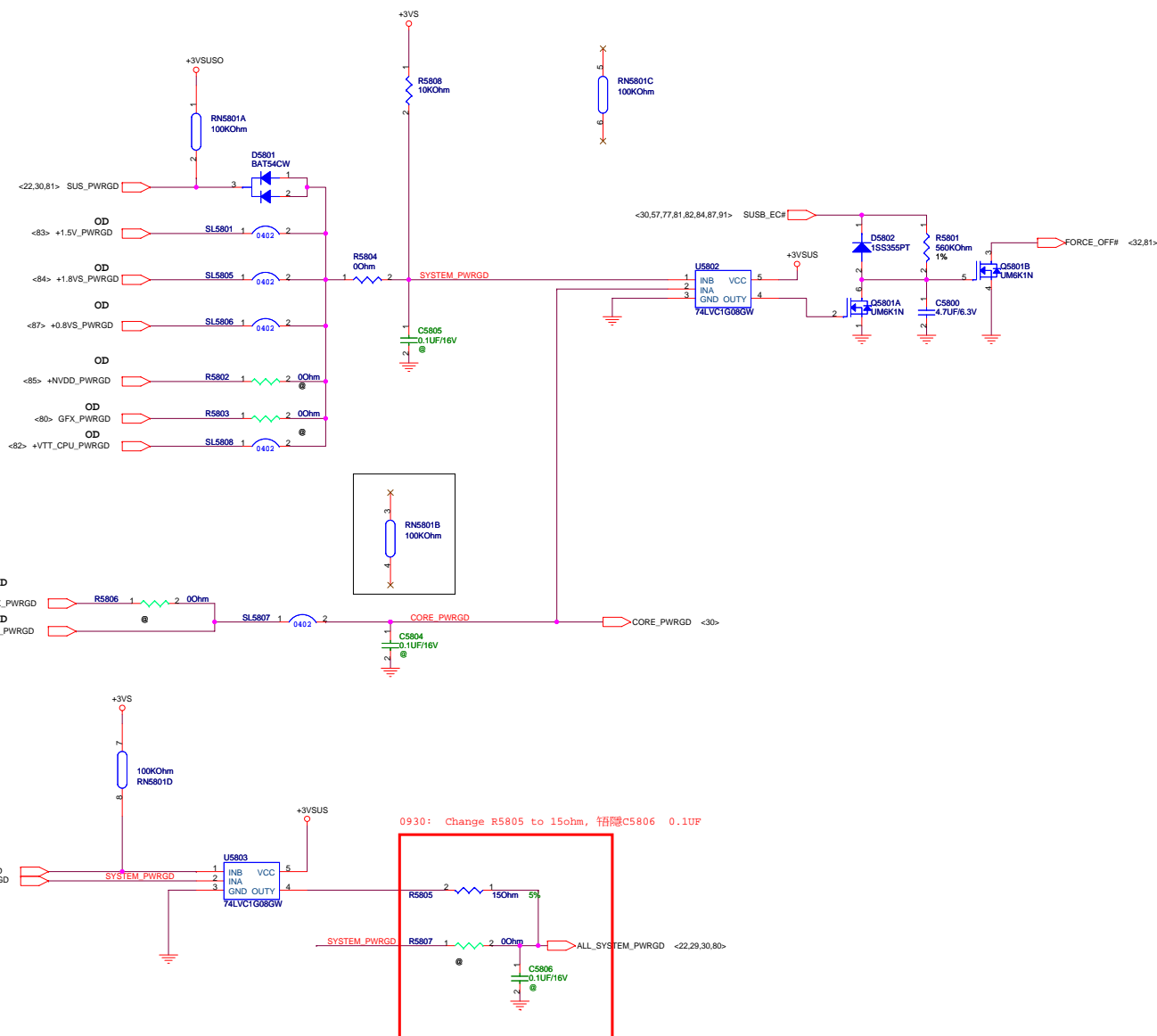
## Power LED









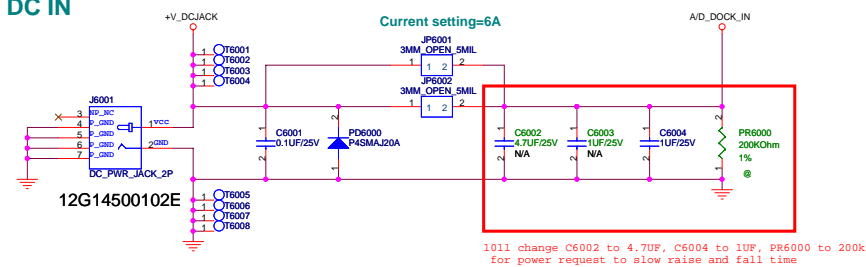




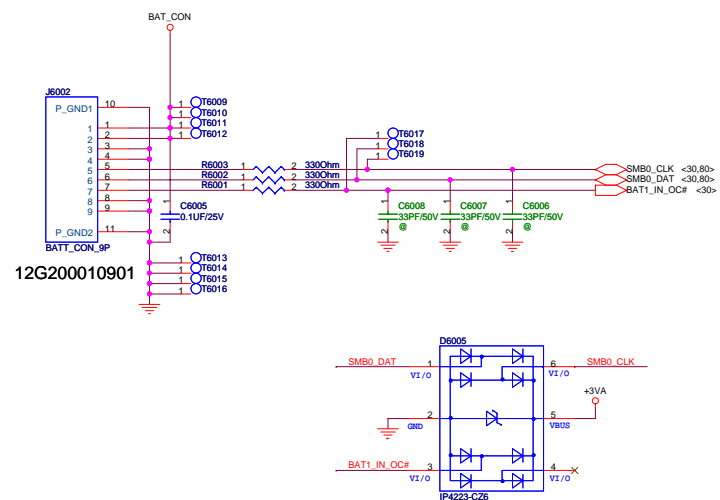




## DC IN



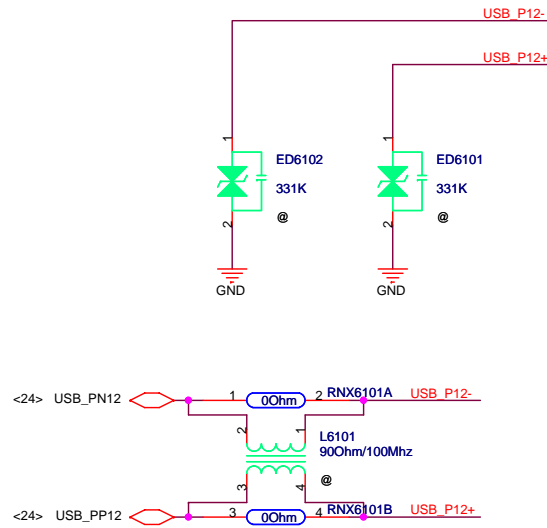
## BAT IN



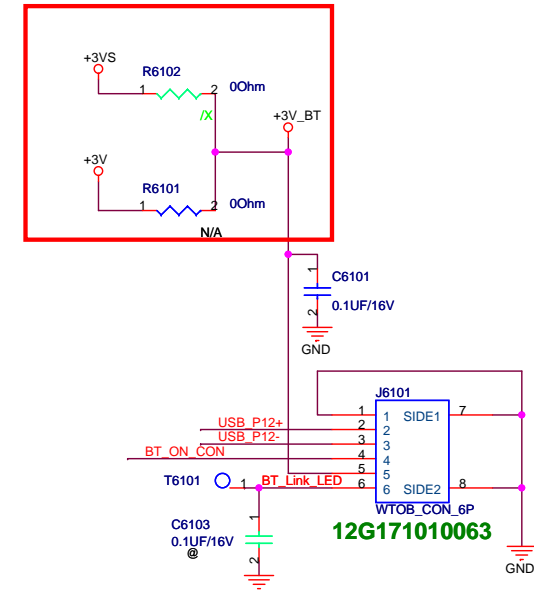


# BLUETOOTH

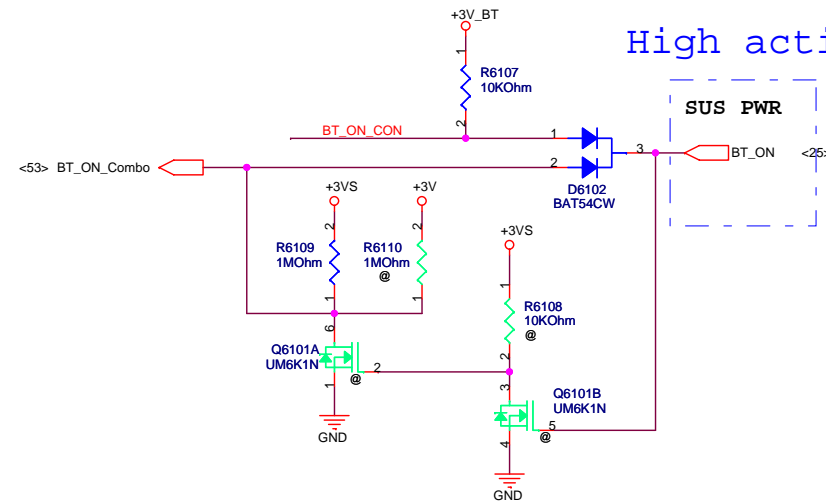
Reserve for EMI



10/12 Reserve R6102 For Energy Satr



High active











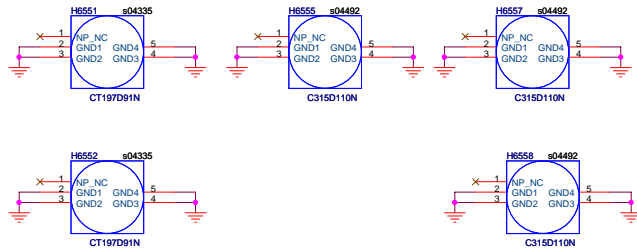




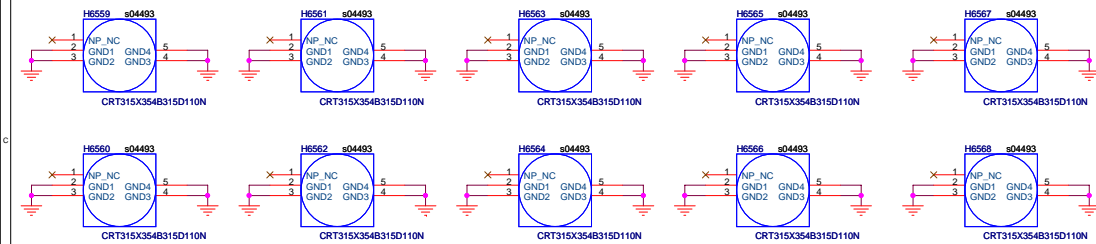
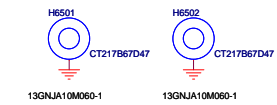
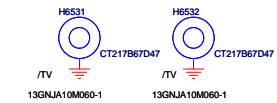


Screw D x 2 for ODD

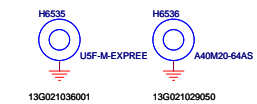
Screw E x 4



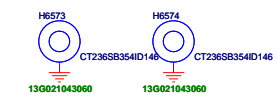
Screw F x 10

MiniCard (Wifi) Stand-Off  
HMCMiniCard (TV) Stand-Off  
MC

## FAN Stand-Off



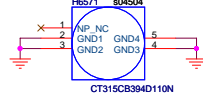
## HDD Stand-Off



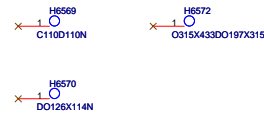
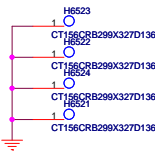
Screw B x 4 CPU Bracket



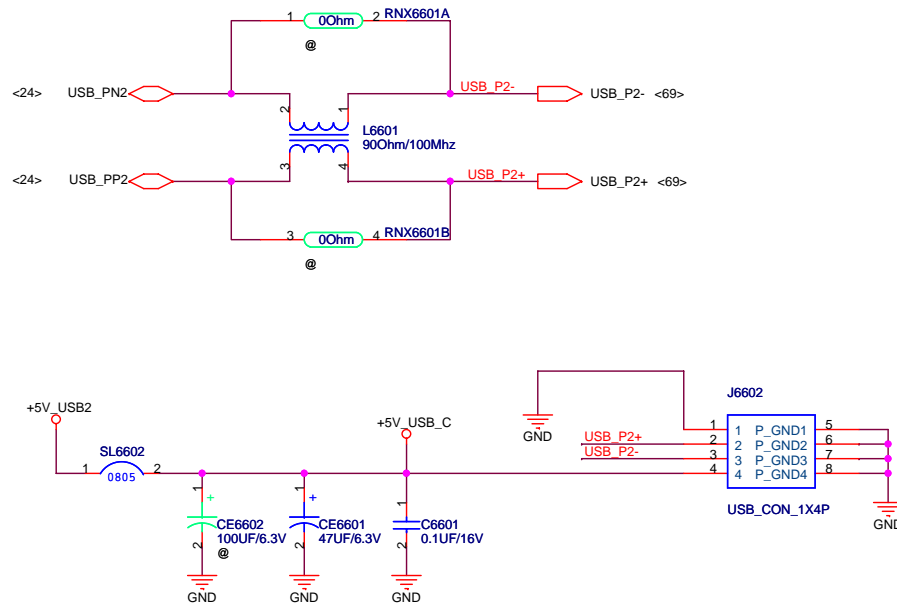
Screw H x 1



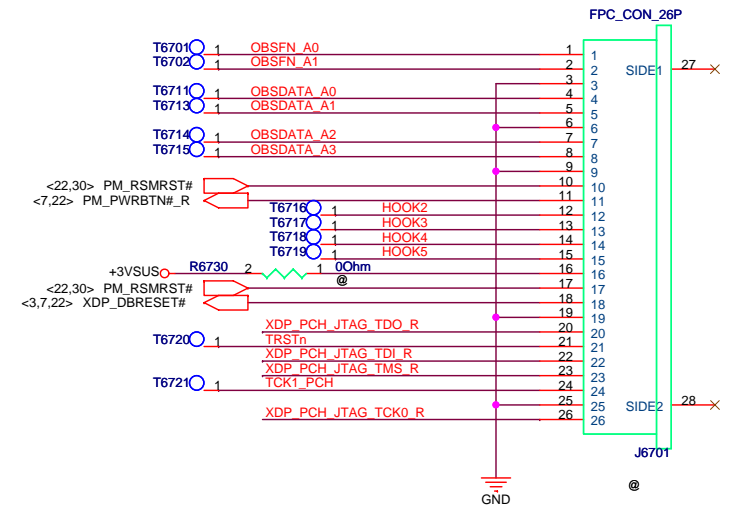
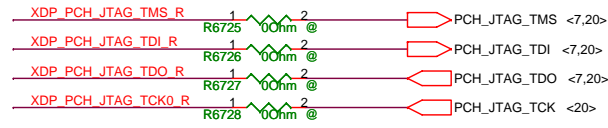
Screw C x 4 GPU Bracket









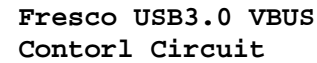
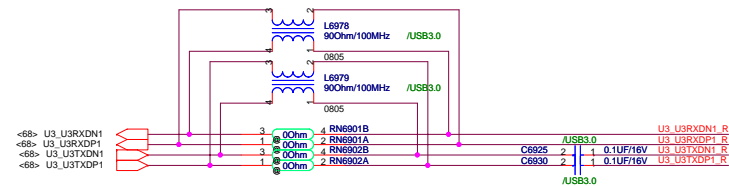
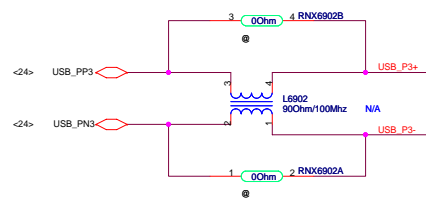




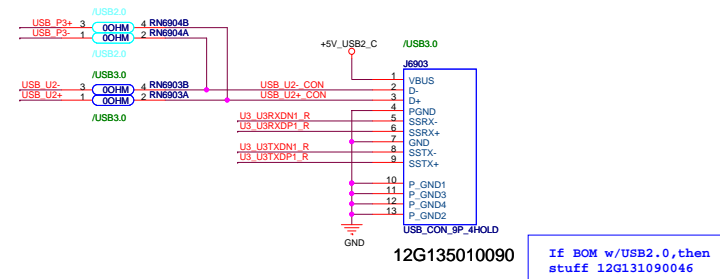




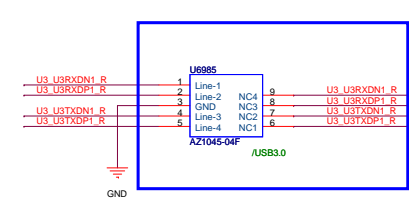
USB3.0  
EMI-Protection



1. Unmount R6819,U6901. Mount F6903,R6903,R6904 for Poly Fuse in Ver. D1 Fresco Chipset IC.
2. Mount R6819,U6901. Unmount F6903,R6903,R6904 for PWR SW in Ver. E0 Fresco Chipset IC.



USB3.0/USB 2.0  
ESD-Protection



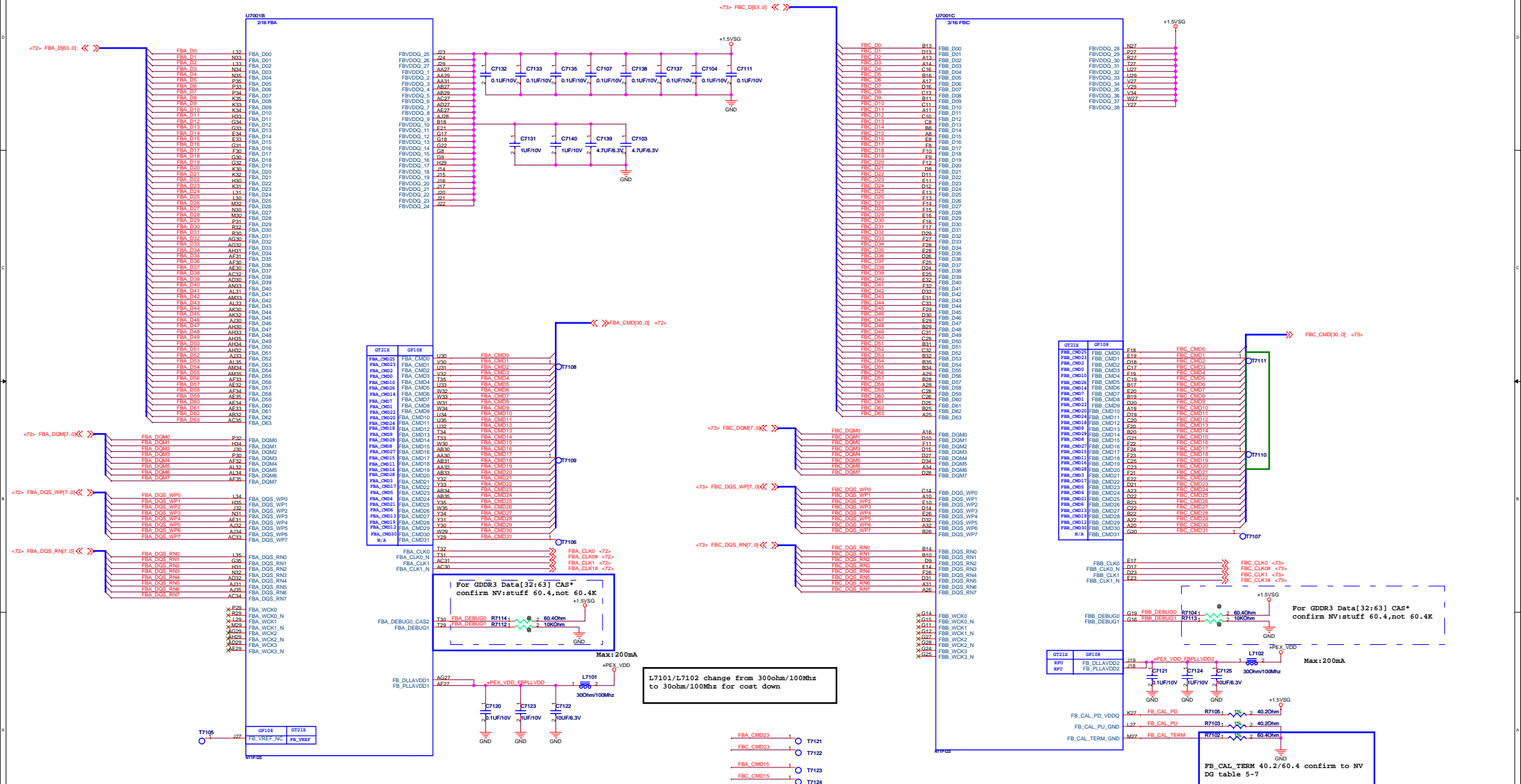






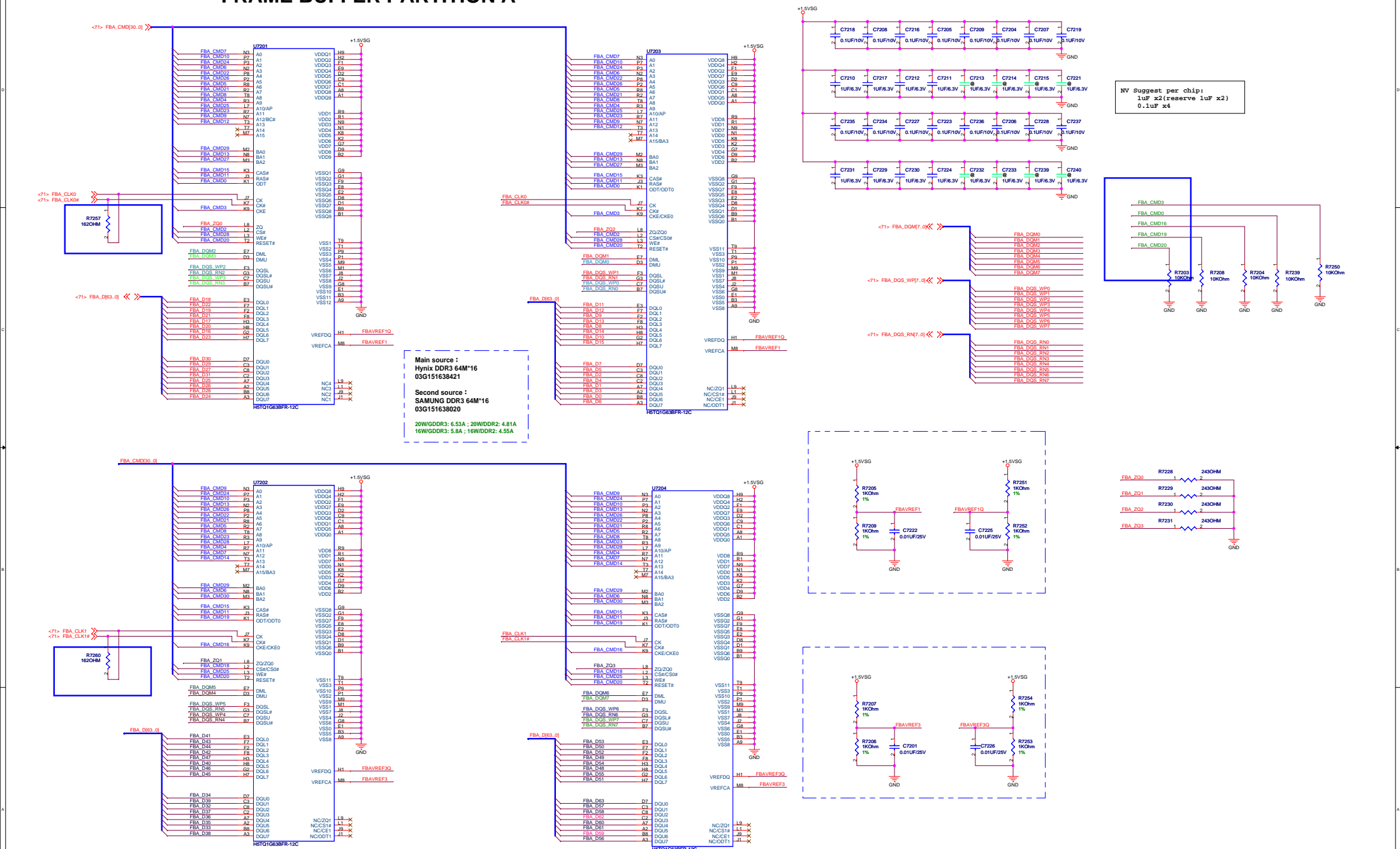
## GPU MEMORY INTERFACE: PARTITION A

## GPU MEMORY INTERFACE: PARTITION C



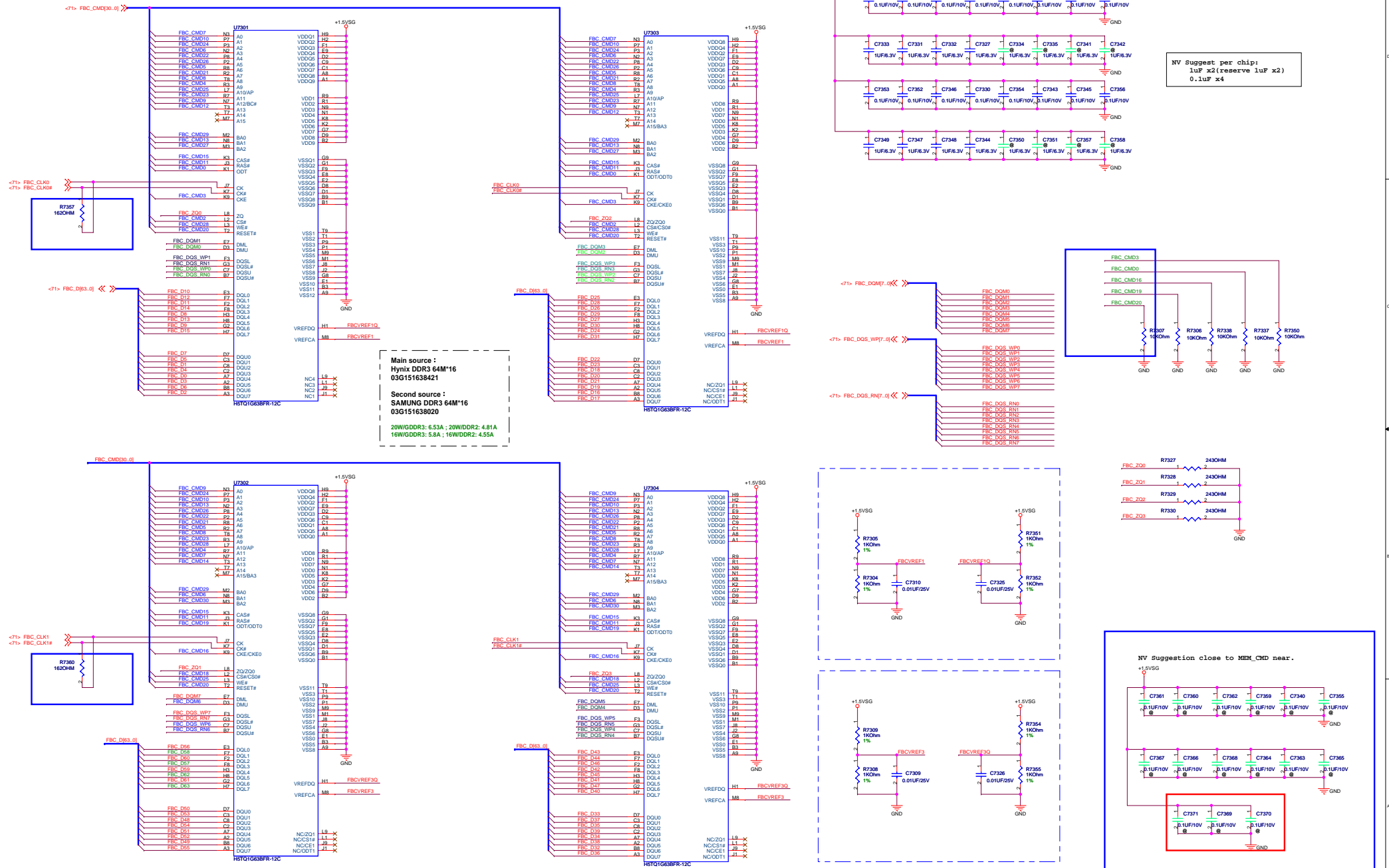


## FRAME BUFFER PARTITION A





## FRAME BUFFER PARTITION C

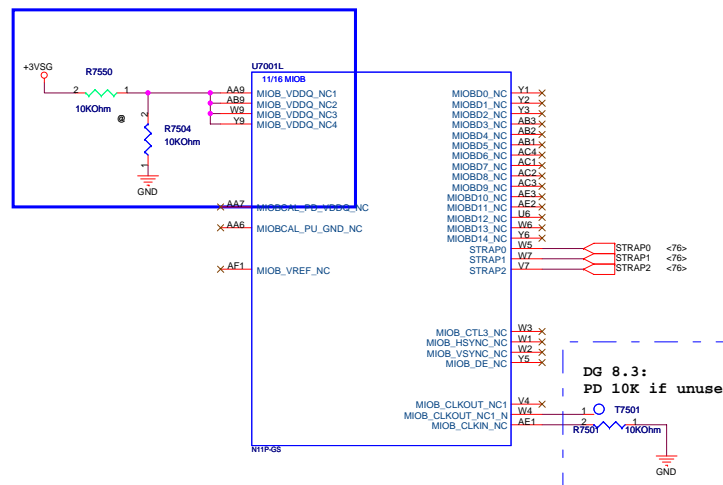
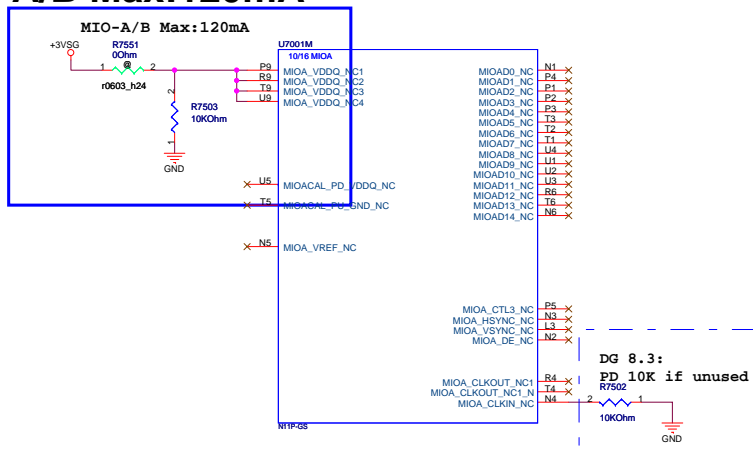








# MIO-A/B Max:120mA



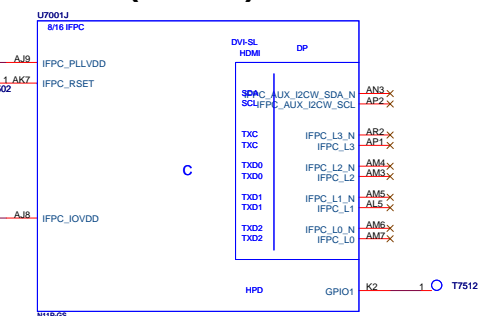
## GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	N/A
1	IN	N/A	IFPC HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVD VID 0
6	OUT	N/A	NVVD VID 1
7	OUT	N/A	NVVD VID 2
8	I/O	LOW	OVER THERMAL
9	I/O	LOW	THERMAL ALERT
10	OUT	N/A	FBVREF SELECT
11	I/O	Low	SLI SYNCO
12	IN	N/A	AC DETECT
13	OUT	N/A	MEM_VID/PWR Control
14	OUT	N/A	PWR Control

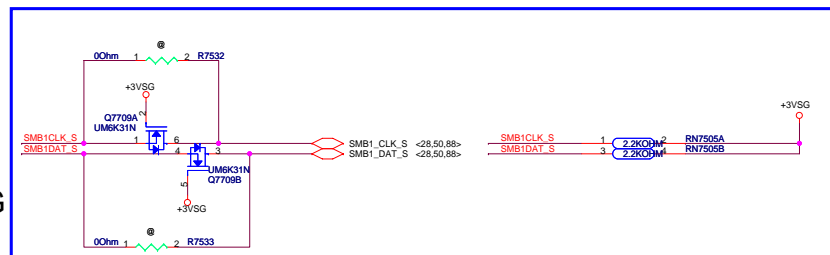
## GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
15	IN	N/A	IFPE HOTPLUG (HDMI)
16	OUT	N/A	FAN PWM CONTROL
17	IN	N/A	RESERVED
18	IN	N/A	RESERVED
19	IN	N/A	IFPD HOTPLUG
20	IN	N/A	RESERVED
21	IN	N/A	IFPF HOTPLUG
22	IN	N/A	SLI Swap Ready Signal
23	I/O	N/A	STEREO

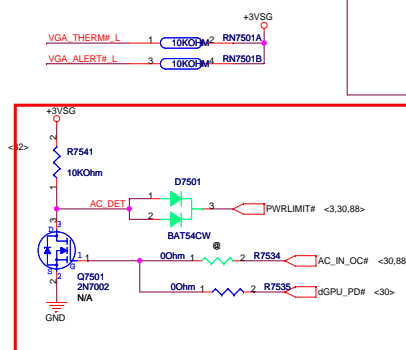
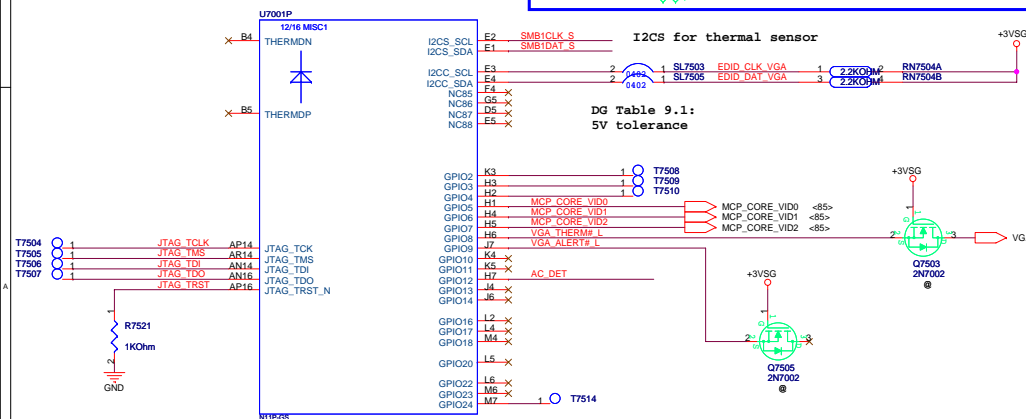
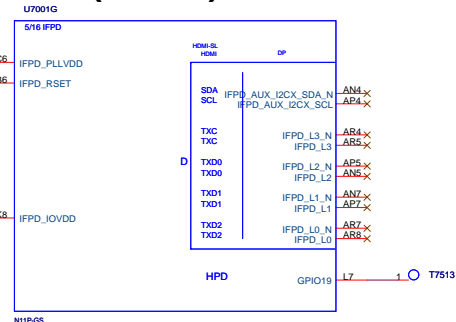
## HDMI(link C)



## GPIO, TEMP SENSOR, JTAG I2C ADDRESS: 0x9AH



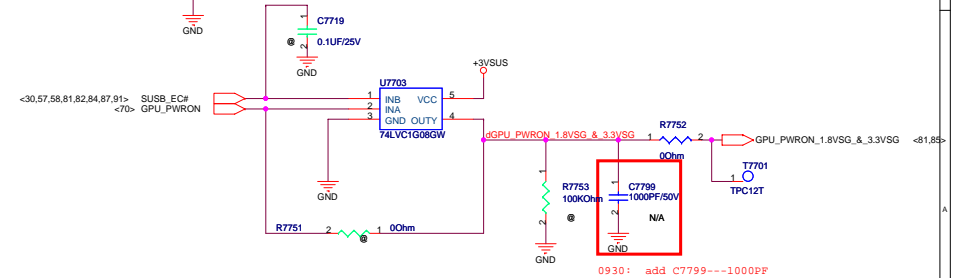
## DVI(link D)















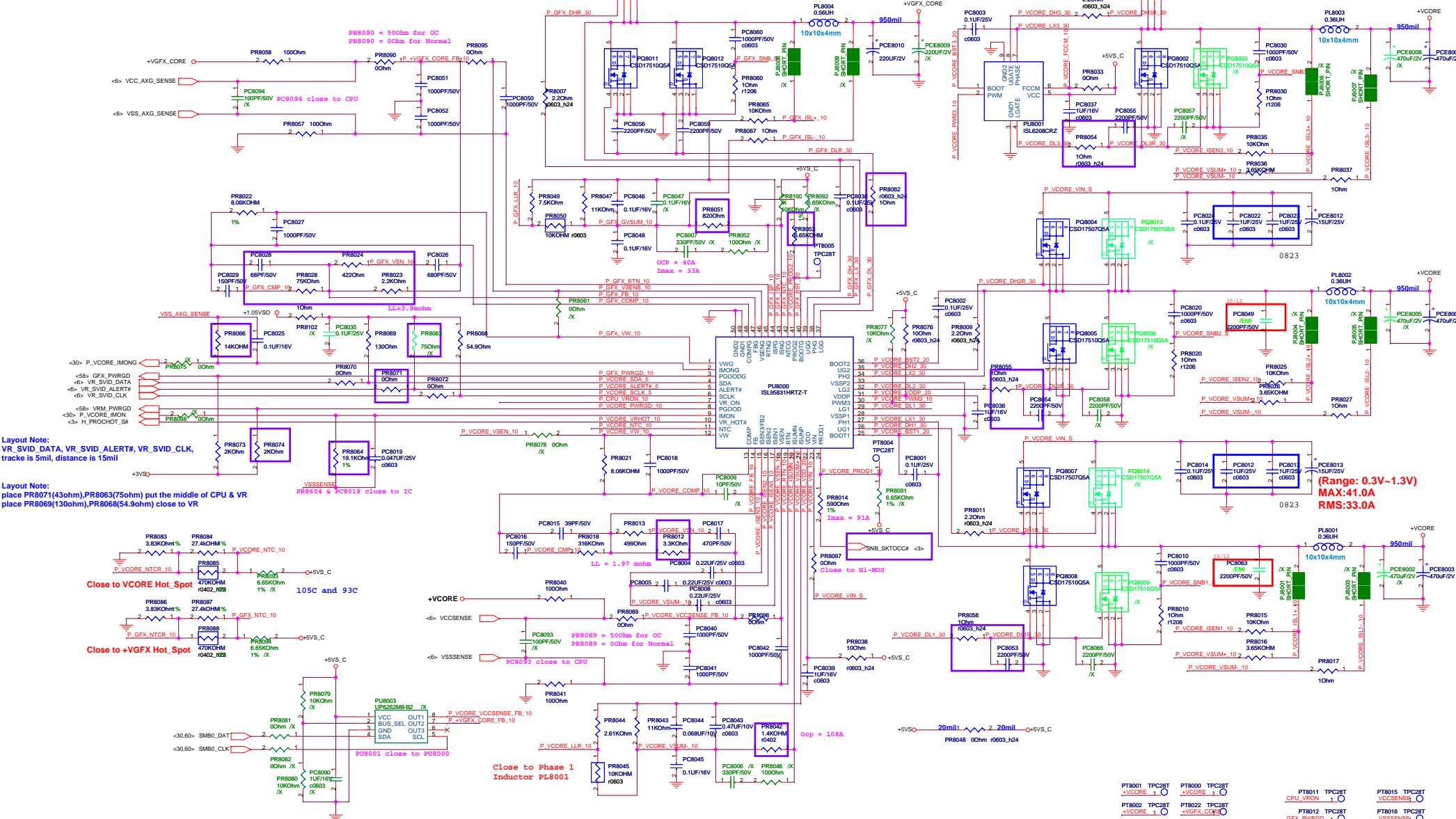
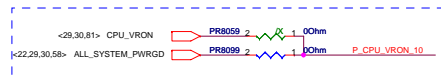


Rev	Date	Description
1.1	2010/08	(1)Page3 & 20 & 70 : CPU socket P/N change to 12G011909893; PCH P/N as 02G010027100; GPU P/N change to 02G190018200; change VRAM to Hynix H5TQ1G63DFR-11C & SAMSUNG/K4W1G1646E-HC11 (2)Page3/80 : link SNB_SKTOCC# to VRM controller (3)Page3 : reserve 0.01uF(C0335/C0336/C0337) for H_CPUPWRGD/PM_SYNC#/H_SNB_INV# (4)Page3/7 : un-link XDP_PREQ# to XDP for saving layout space, and add test point on XDP connector side. (5)Page6 : change +VDDQ power source from +1.5VS to +1.5V, so delete JP0601&JP0602 (6)Page6/80 : add R0602 serial R & R0605 pull-up R for VR_SVID_ALERT#, and change PR8071 to 0ohm, un-mount PR8063 (7)Page6 : un-mount CE0601 for factory DFM (8)Page26/27 : change SL0402 to SL0603 for SL2601/SL2602/SL2603/SL2702/SL2703/SL2708/SL2710/SL2711/SL2712/SL2717/SL2718/SL2719 (9)Page29 : un-mount Clock Gen. & others interrelated components (10)Page30 : 10.1 change net name from FAN_PWM to FAN0_PWM(page 50) 10.2 DSW_WAKE# changed to no function 10.3 PM_EXTTTS#0 changed to no function 10.4 changed net name from RFON_SW# to RF_SW#(page 53) 10.5 OP_SD# changed from GPC5 to GPE0, and VOLUME_LED# changed from GPE0 to GPE3 10.6 THRO_CPU change from GPE5 to GPH1, and changed net name from THRO_CPU to THRO_CPU#,and correct THRO_CPU# control, R0307 changed from 62ohm to 200ohm(page 3); 10.7 PM_SLP_SUS# changed to no function (11)Page33 : delete +3VS power & SL3310 for LAN chip changed to AR8151 (12)Page33 : un-mount C3302 for BUF_PLT_RST# glitch issue (13)Page36 : change C3631 from 1UF/10V to 2.2UF/10V for EA test failed (14)Page36/20 : change DVDD_IO power source to +3VSUS, and then un-mount U2002 & R2028 and stuff R2024 (15)Page37 : ex-change MUTE_POP# & AMP_SHD# MOS (16)Page42 : change the Card Reader chip to AU6437-GDL (17)Page44 : change J4401 to JDEBUG1 for BU request (18)Page46 : unstuff C4602/C4604/C4606 for EA test failed (19)Page68 : change FRESCO FL1000G (D1) TFBGA100 (MP) to FRESCO FL1000G (E0) TFBGA100 (ES) (20)Page66/69 : change CE6602 & CE6932 to c3528 size (21)Page76 : change R7627 value for N12P-GS and pay attention to R7618 value (22)Page77 : change Q7702 to CSD17507Q5A for high Rdson (23)Page77 : change R7703 to 0ohm (24)Page55 : mount stlitich Caps EC5513~EC5516, and delete EC5512 (25)Page : change RNX4501 ~ RNX5302 ~ RNX5401 ~ RNX6101 ~ RNX6601 ~ RNX6902 ~ RN6901 ~ RN6902 from 0402 size to 0603 size (26)Page6 : un-mount CE0601 for factory DFM (27)Page26 : reserve CE2601 for +1.05VS (28)Page68 : add R6801 for GPIO "USB3_SMI#"

Rev	Date	Description
2.0	2010/09/30	1: Page 69, USB 2.0 mount F6903 & R6903 2 USB 3.0 mount F6903 & F6904, un-mount R6903 2 : Page 68, unmount R6813 3 : Page 45, Mount R4506, increase Q4502 Vgs 4 : Page 20, Mount R2008 for ME firmware update 5 : Page 85, Change PR8556 to 91K, Change C7716 to 0.22UF and add D8501 for discharge 6 : Page 20, Mount R2008 for ME firmware update 7 : Page 77, Change R7705 to 47K, Change C7718 to 0.22UF 8 : Page 6, R0617, R0618 Change to 1K 9 : Page 82, Change PR8201 to 360K, Change PC8201 to 0.01UF 10 : Page 77, Add C7799---1000PF 11 : Page 58, Change R5805 to 15ohm, reserve C5806 0.1UF 12 : Page 70, Change GPU to N12PJ 02G190018204 13 : Page 38, Change J3802 to 12G14030108N 14 : Page 20, Change PCH to 02G010027500 15 : Page 68, Change C6809 to 4.7UF 16 : Page 57, Change R5719 to 100ohm for quick discharge 17 : Page 17,14, add pull up R1701, R1401 18 : Page 44, JDEBUG connector Power change to +3VS 19 : Page 70/77,change U7002 & U7703 from NC7S208P5X_NL to 74LVC1G08GW for saving the variety of component. 20 : Page 80, un-stuff PCE8008 , mount PCE8007
	2010/10/06	21 : Page 48, For EMI, mount L4801, L4802, L4803, L4804,un-mount RN4801, RN4802, RN4803, RN4804 22 : Page 30, Change GPE1 to dGPU_PD#, Change GPE5 to MEDIA_KEY_LED# 23 : Page 75, Add D7501 for PWRLIMIT#
	2010/10/07	24 : Page 56, For EC +3v reference, mount R5601 R5610 Q5601 Q5602---> change it back (2010/10/11) 25 : Page 30, FOR ITE Suggestion, Change R3007 form 43k to 0ohm 26 : Page 30, Change SL3010 to R3009 0ohm prevent EC version change. 27 : Page 07, un-mount XDP: J0701, R0701, R0702 , R0703, R0704, R0705, RNX0702 28 : Page 30, add battery discharge power limit circuit
	2010/10/09	29 : Page 06, change +1.5V to +1.5VS for energy star 30 : Page 42, Reserve R4218 (+3VS) for energy star 31 : Page 31, SL3101 change to R3101 330 OHM for energy star 32 : Page 56, change R5620 R5613 to 1k for energy star 32 : Page 68, Reserve +3VS for USB3.0 for energy star and remove JP6801 JP6802 JP6803
	2010/10/11	33 : Page 60, Change C6002 to 4.7UF, C6004 to 1UF, PR6000 to 200k for power request to slow raise and fall time 34 : Page 91, Change PQ9113 to 07G005B19010 for large current 35 : Page 37, Reserve C3725 C3726 C3727 C3728 FOR EMI
	2010/10/12	36 : Page 61, Reserve R6102 For Energy Satr 37 : Page 45, Add R4513 to change J4502 PIN5 from GND_AUDIO to GND 38 : Page 60, mount C6002 C6003 for POWER suggestion 39 : update power circuit for BOM 40 : Page 37 Page 03, unmount R3715 Q3704 C3711 R0303
	2010/10/13	41 : Page 69, reserve R6905 for leakage, If USB3.0 choose +3VS for Energy Star, mount F6905 un-mount F6904 42 : Page 03, Mount Q0302 R0335 For DRAMPWROK quick discharge 43 : Page 69, Change F6904 F6905 from 07G012200130 to 07G014200020 43 : Page 37, For EMI request, Change jump to bead (L3703, L3704, L3705, L3706)



## IMVP7 CPU VCORE REGULATOR



- |  |  |  |
|--|--|--|
| <b>IP Current:</b><br>$I_{in} = V_o/I_o(0.75 * V_{in}) = 3.9A$ | <b>3. Voltage &amp; Current:</b><br>$0.3V - 1.3V : 55A$  | <b>5. Frequency:</b><br>$R_{fset} = (T - 0.29) * 2.65$<br><b>Frequency= 300KHZ</b> |
| <b>Ripple Current:</b><br>$I_{ripple} = 7A$                    | <b>4.ripple voltage:</b><br>$I_{peak} = (v_{in} - v_o) * D / (L * F_{sw}) = 8.8A$<br>$ESR = 9/3 = 3mohm$<br>$V = 26.4mV$ |  |

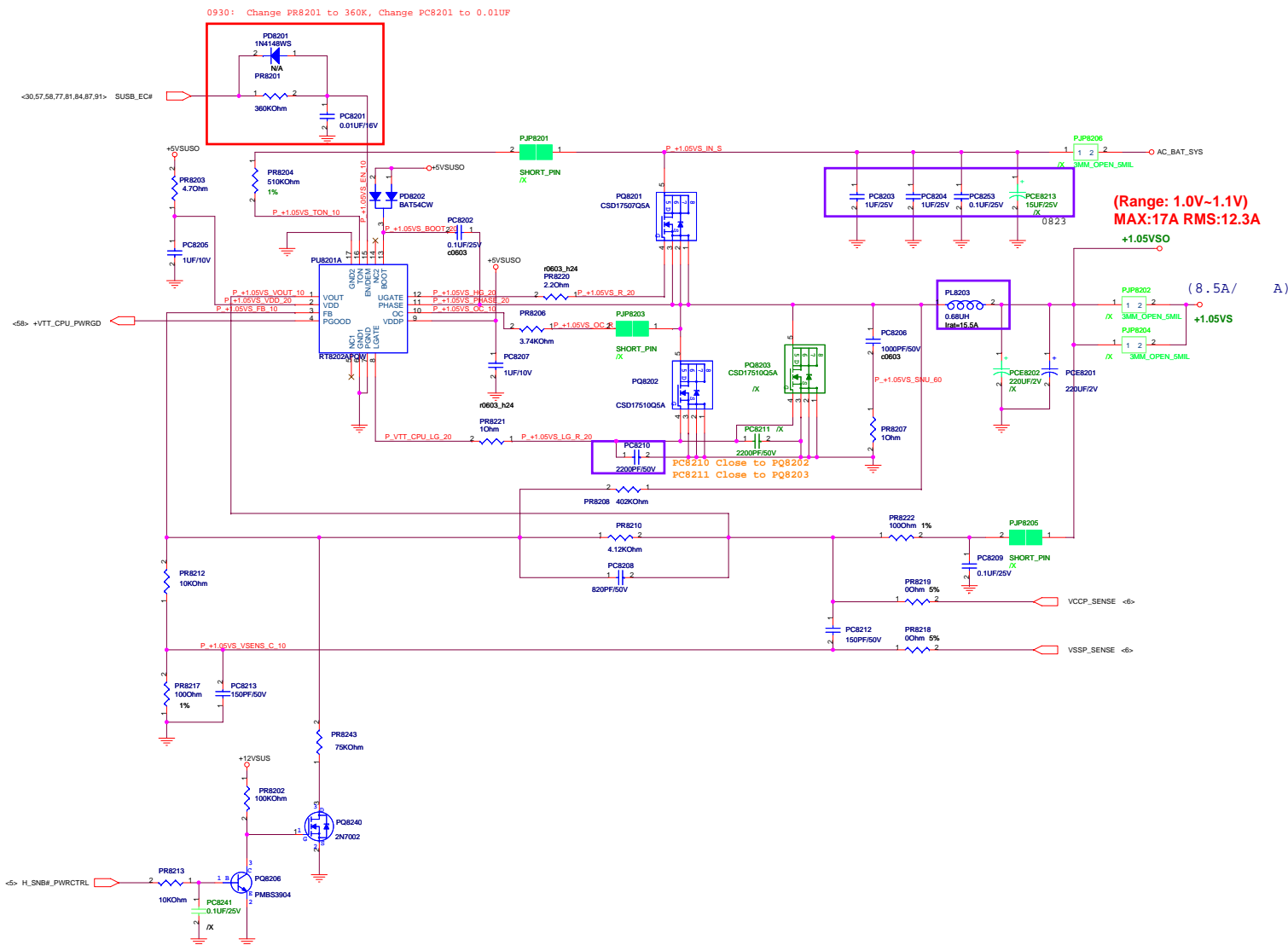
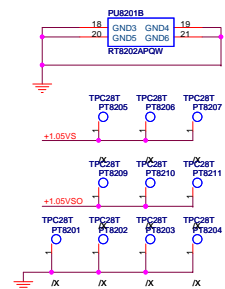
For 35W CPU:  
PR8014 = 5.62K for Vboot=0V/49A; PR8053 = 9.53K for 105C/25A  
For 45W CPUs:  
PR8014 = 590Ohm for Vboot=0V/91A; PR8053 = 6.65K for 105C/33A

PT8001	TPC28T	PT8000	TPC28T		PT8011	TPC28T	PT8010	TPC28T
+VCORE	1	+VCORE	1		CPU_VRON	1	+VSENSEN	1
PT8002	TPC28T	PT8002	TPC28T		PT8012	TPC28T	PT8016	TPC28T
+VCORE	1	+VGFV_CORE	1		GFV_PWRGRD	1	+VSENSEN	1
PT8003	TPC28T	PT8023	TPC28T		PT8013	TPC28T	PT8017	TPC28T
+VCORE	1	+VGFV_CORE	1		VRM_PWRGRD	1	SVS_C	1
PT8018	TPC28T	PT8024	TPC28T					
GND	1	+VGFV_CORE	1					
PT8019	TPC28T	PT8026	TPC28T					
GND	1	GND	1					
PT8020	TPC28T	PT8027	TPC28T					
GND	1	GND	1					
PT8025	TPC28T	PT8021	TPC28T					









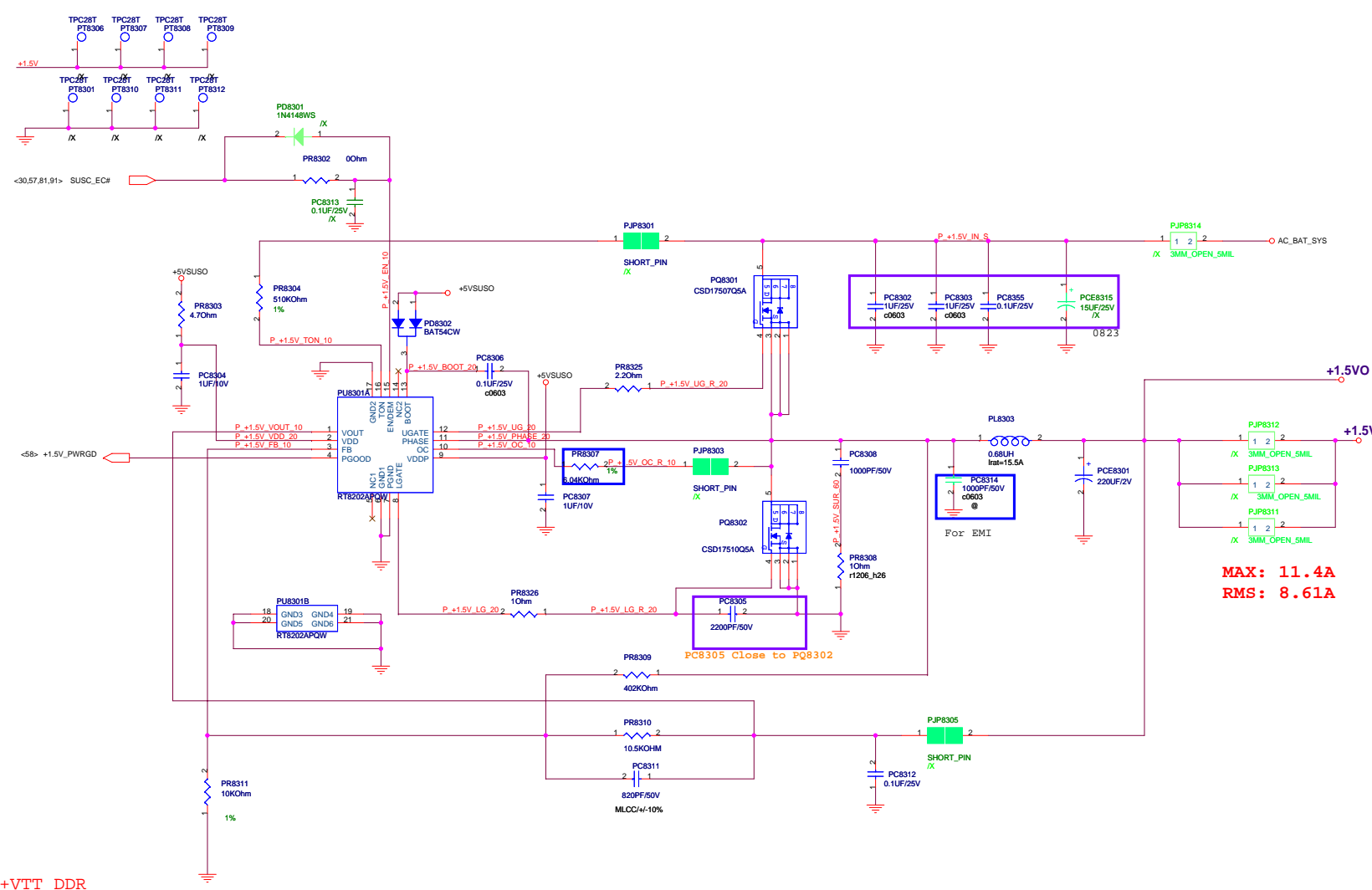
### Power information

1. I/P Current:  
 $I_{in} = V_o / (0.75 \cdot V_{in}) = 2.1A$
2. Ripple Current:  
 $I_{ripple} = 5A$
3. Dynamic:  
 $I_{peak} = 1.98A$   
 $DCR = 3.3m\Omega$   
 $V = 6.534mV$

1. Voltage & Current:  
 $+V_{TT\_CPU}: 1.05V @ 25A$
2. Frequency:  
 $Ton = 3.85pRt(on)/Vin - 0.5 = 0.3us$   
Frequency =  $Vout/(Vin * Ton)$   
= 500KHZ
3. OCP:  
Set  $PR8206 = 3.74K\Omega$   
 $I_{ocp} = R_{ocp} * 20/R_{ds(on)} = 27.2A$

<b>H_VTTVID1</b>	<b>+VTT_CPU</b>
<b>1</b>	<b>1.05V</b>
<b>0</b>	<b>1.1V</b>





**Power information**

1. **IP Current:**  
 $I_{in} = V_o I_o / (0.75 \cdot V_{in}) = 3.6A$

2. **Ripple Current:**  
 $I_{ripple} = 5A$

3. **ripple voltage:**  
 $I_{peak} = (V_{in} - V_o) \cdot D / (L \cdot F_{sw}) = 2.07A$   
 $DCR = 10m\Omega$   
 $V = 20.7mV$

1. **Voltage & Current:**  
 $1.5V: 16.45A$

2. **Frequency:**  
 $T_{on} = 3.85p \cdot R_t(on) / (V_{in} - 0.5V) = 0.3\mu s$   
 $Frequency = V_{out} / (V_{in} \cdot T_{on}) = 500KHz$

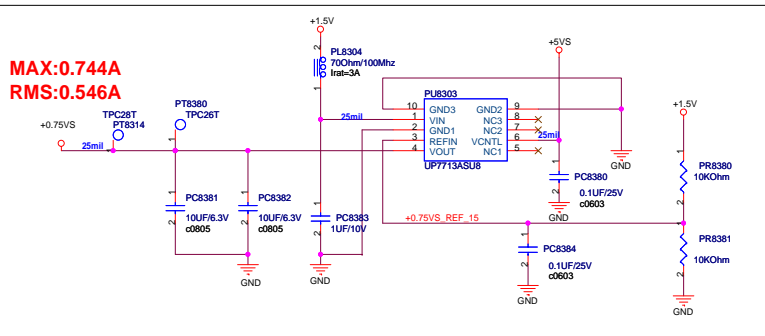
3. **OCp:**  
Set PR8307=4.7k $\Omega$   
 $I_{ocp} = R_{ocp} \cdot 20 / R_{ds(on)} = 17A$

4. **Soft start time:**  
Soft-Star duration is 1.35ms

5. **Inrush Current:**  
 $C_{total} = 220\mu F$   
 $I_{inrush} = 0.163A$

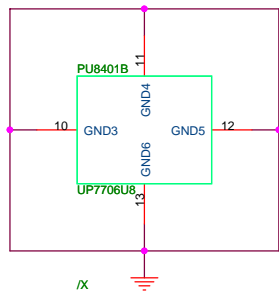
**MAX: 11.4A**  
**RMS: 8.61A**

+VTT\_DDR



**MAX:0.744A**  
**RMS:0.546A**





1.8VS @ 0.7A

### 1. Dropout Voltage:

$\Delta V = 0.3V$  ( $I_o = 2A$ )

### 2. Current Limit:

$I_{limit} = 3A$

### 3. Continue Current:

$I_{cont} = 1A$

### 4. Power Dissipation:

$R_{thjc} = 250^{\circ}C/W$

$P_d = 0.4W$

### 5. EN Voltage:

$V_{rising} = 2V$

$V_{falling} = 0.8V$

### 6. Supply Voltage:

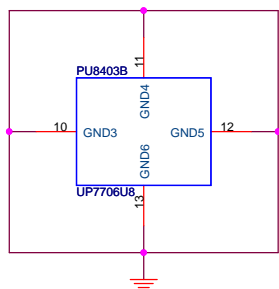
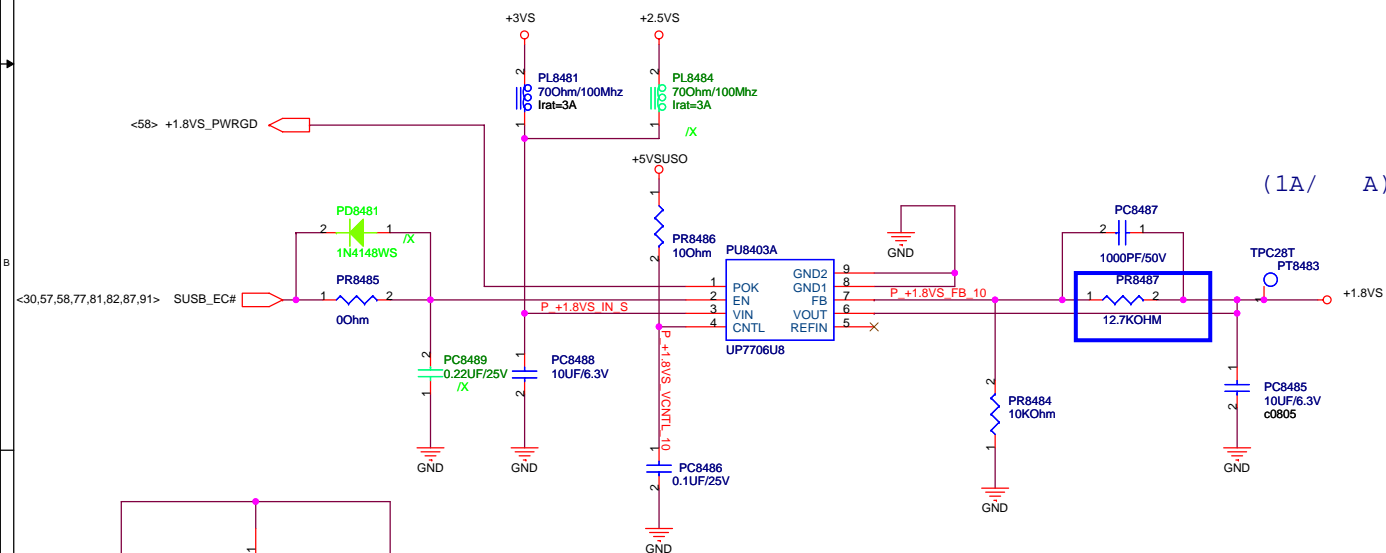
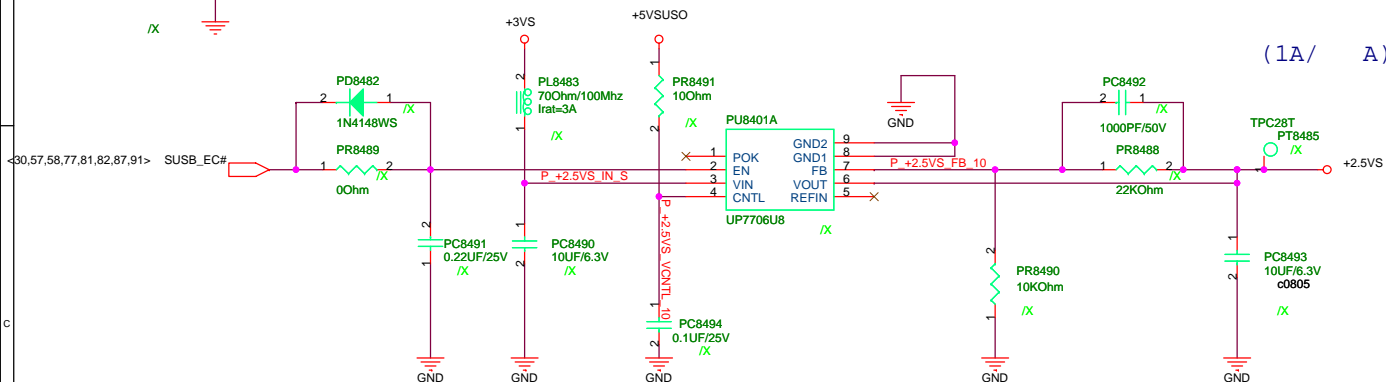
$V_{cc} = 3V$

### 7. Inrush current:

$T_{ss} = 400\mu s$

$C_{total} = 10\mu F$

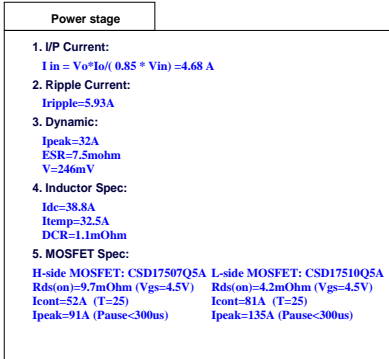
$I_{inrush} = 0.063A$



<Variant Name>

<b>ASUS</b>		Title : +1.8VS	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
A3		1.0	
Date: Wednesday, October 13, 2010		Sheet 84 of 92	





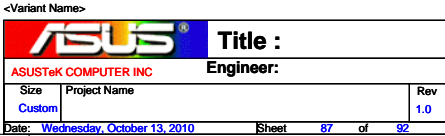
Controller	
1. Voltage & Current:	+VGA_Core=0.875V/41A
2. Frequency:	CCM:Fsw=300*33/RFS=300KHZ
3. OCP:	Vocset=25*Ilim*I <sub>Rsense</sub> Ilim=30*2=60A
4. Slew rate:	Slewrate=Iss/PC/7810=100uA/10nF=10mV/uS
5.Inrush Current:	C total = 440 uF I inrush= 0.3 A
6.Droop Resistance:	Rdroop=R1/R2*10 <sup>6</sup> Rsense=0.39mohm





		Title :	
ASUSTek COMPUTER INC. NB3		Engineer:	
Size	Project Name	Rev	
A2	Design IP	1.0	
Date: Wednesday, October 13, 2010		Sheet	86 of 92














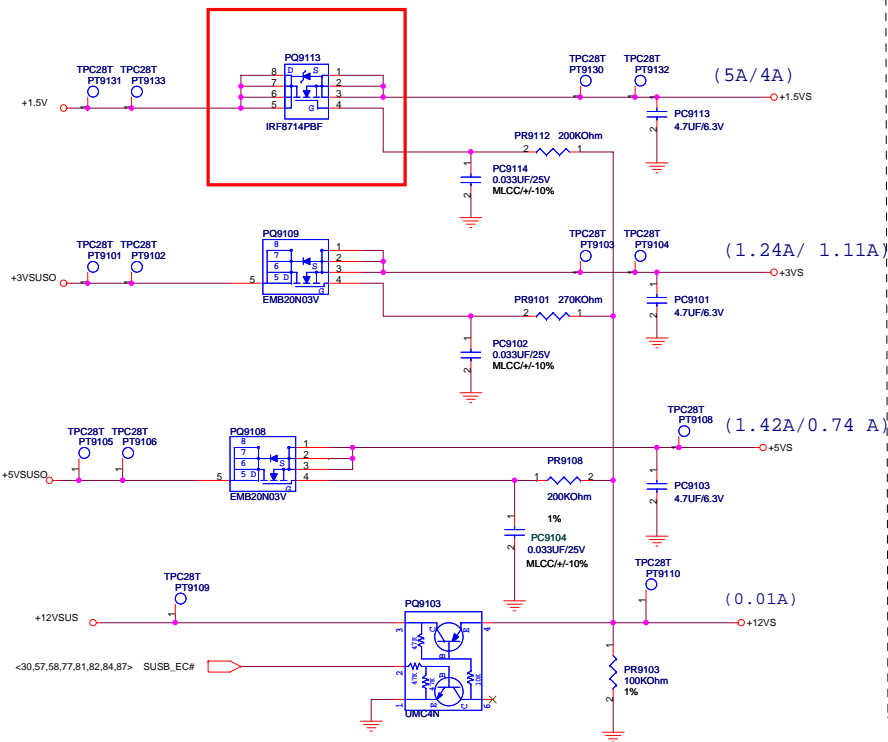


	5	4	3	2	1						
D					D						
C					C						
B					B						
A					A						
					<div><div></div><div>Title :</div></div>						
					<div><div>ASUSTeK COMPUTER INC. NB3</div><div>Engineer:</div></div>						
					<table><tr><td>Size</td><td>Project Name</td><td>Rev</td></tr><tr><td>A</td><td>Design_IP</td><td>1.0</td></tr></table>	Size	Project Name	Rev	A	Design_IP	1.0
Size	Project Name	Rev									
A	Design_IP	1.0									
					<div><div>Date: Wednesday, October 13, 2010</div><div>Sheet 90 of 92</div></div>						

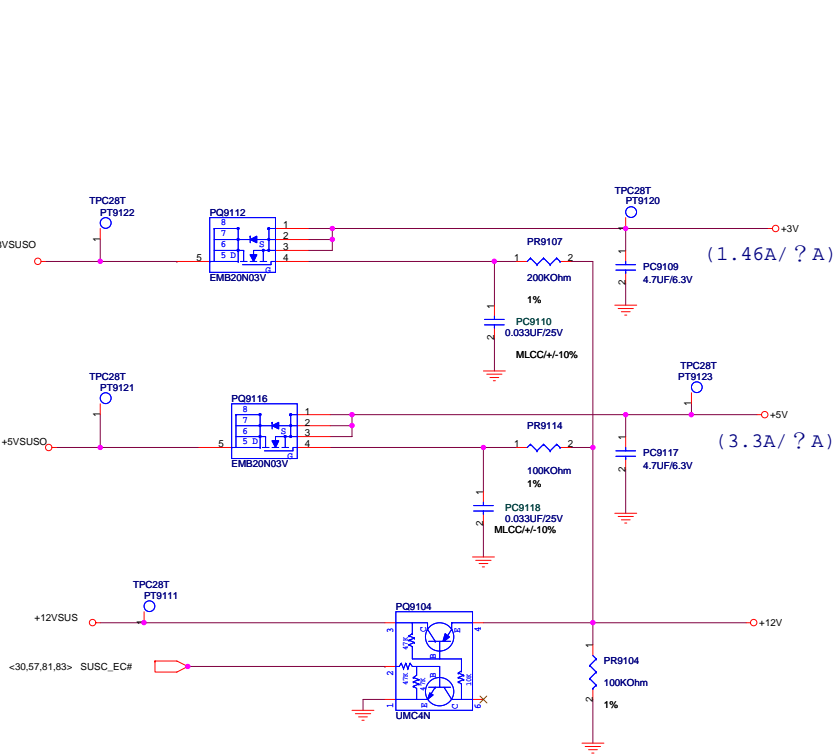
WWW.AliSaler.Com



SUSB#\_PWR POWER



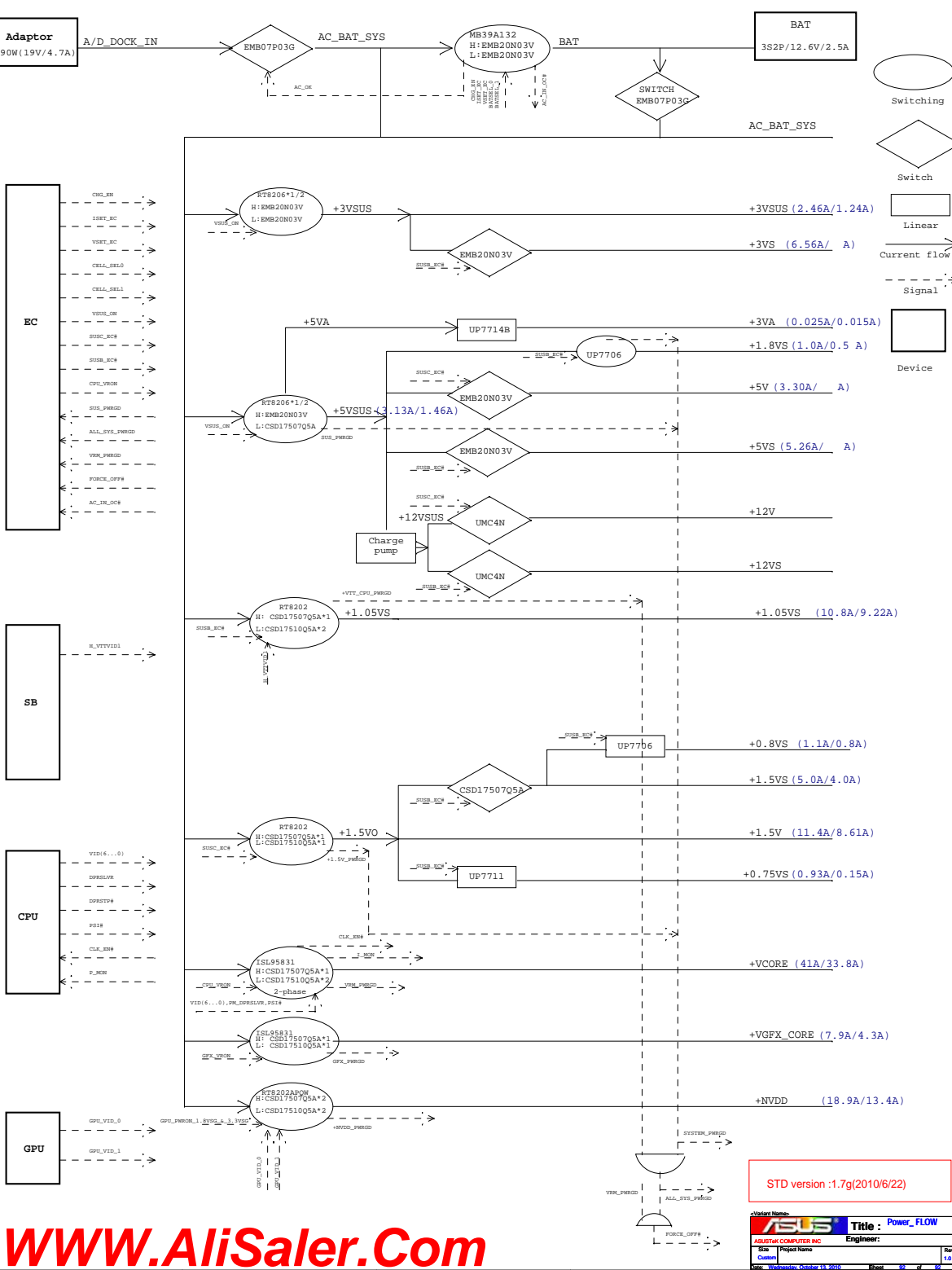
SUSC#\_PWR POWER



<Variant Name>









## U53 Power On Sequence Diagram Rev.0.14





AC-IN Mode

- 1 +3VA/+5VA/+3VA\_EC
- 2 EC\_RST#  
VccDSW
- 3 PM\_SLP\_SUS#
- 4 PM\_DPWROK
- 5 VSUS\_ON  
+3VSUS/+5VSUS  
SUS\_PWRGD
- 7 ME\_SusPwrDnAck
- 8 PM\_RSMRST#
- 9 ME\_AC\_PRESENT
- 10 PM\_SUSACK#
- 11 PWR\_SW#
- 12 PM\_PWRBTN#
- 13(a) PM\_ME\_SLP\_LAN#
- 13(b) PM\_ME\_SLP\_A#
- 14 PM\_SUSC#
- 15 PM\_SUSB#
- 16 SUSC\_EC#  
+1.5V/+3V/+5V
- 17 SUSB\_EC#  
+0.8VS/+0.75VS/+1.5VS//+1.8VS/+3VS/+5VS  
+PEX\_VDD/+1.5VSG/+1.8VSG/+3VSG/+NVDD
- 20 SYSTEM\_PWRGD  
+VTT\_CPU
- 21 +VTT\_CPU\_PWRGD  
+0.8VS
- 22 +0.8VS\_PWRGD
- 23 ALL\_SYSTEM\_PWRGD
- 24 PM\_PCHPWROK
- 25 PM\_SYSPWROK
- 26 H\_DRAM\_PWRGD
- 27 H\_CPUPWRGD
- 28 SVID  
+VCORE
- +VccGFX
- 29 VRM\_PWRGD
- 30 SUS\_SATA#
- 31 BUF\_PLT\_RST#

